InnoSwitch3-AQ Family

CV/CC Valley Switching DCM/CCM Flyback Switcher IC with Integrated 750 V / 900 V / 1700 V Switch for Automotive Applications

Product Highlights

Highly Integrated, Compact Footprint

- Up to 95% efficient across load range
- Incorporates a multi-mode Valley Switching DCM/ CCM flyback controller, 750 V, 900 V or 1700 V switch and secondary-side sensing
- Integrated FluxLink™, feedback link providing reinforced isolation
- 30 V to >1200 VDC input voltage

EcoSmart™ – Energy Efficient

- Less than 15 mW no-load input power

Advanced Protection / Safety Features

- Auto-restart response for output overvoltage and over-current faults
- Accurate programmable output over-current threshold
- Programmable input undervoltage

Full Safety and Regulatory Compliance

- SEooC Class II acc. to ISO 26262
- AEC-Q100 qualified
- Fab, assembly and test sites are IATF16949 certified
- Reinforced isolation per IEC60664-1
- Isolation voltage withstand >4000 V_{RMS}
- 100% production HIPOT testing
- UL1577 isolation voltage 4000 VAC (max), TUV (EN62368-1), CQC (GB4943.1) safety approved. (See Note 3)
- EN IEC 60747-17 (VDE 0884-17) approved. Excellent noise immunity enables designs that achieve class "A" performance criteria for EN61000-4 suite; EN61000-4-2, 4-3 (30 V/m), 4-4, 4-5, 4-6, 4-8 (100 A/m) and 4-9 (1000 A/m), FMC1278 (RI-115)

Green Package

- Halogen free and RoHS compliant

Applications

Power supplies for automotive subsystems such as the traction inverter emergency power supply (EPS), high-voltage to low voltage DC/DC converters (µDCDC) in battery management systems, on-board chargers and 12 V system standby power supplies.

Description

The InnoSwitch™3-AQ family of ICs dramatically simplifies the design and manufacture of isolated flyback power converters in automotive applications. The InnoSwitch3-AQ family combines primary and secondary controllers and safety-rated feedback into a single IC allowing accurate output voltage regulation even with a very wide input voltage range.

InnoSwitch3-AQ family devices incorporate multiple protection features including line overvoltage and undervoltage protection, output overvoltage, over-current limiting, and over-temperature shutdown. Device start-up from 30 V makes InnoSwitch3-AQ parts ideal for emergency power supplies (EPS).

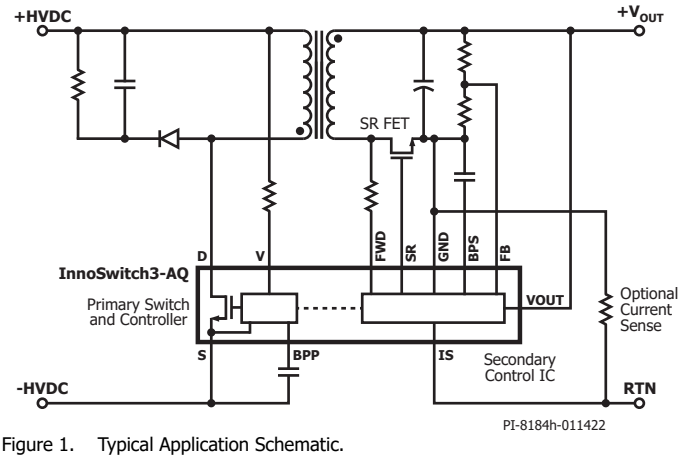


Figure 1. Typical Application Schematic.

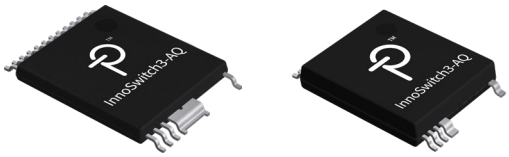


Figure 2. Safety-Compliant InSOP-24D and InSOP-T28G Packages Provide Extended Creepage and Clearance.

Output Power Table

Product[2]	Maximum Recommended Input DC Rail	Output Power (W) At Working Voltage[1]			
750 V MOSFET		30 VDC	60 VDC	400 VDC	800 VDC
INN3977CQ	520 V	10	20	30	–
900 V MOSFET		30 VDC	60 VDC	400 VDC	800 VDC
INN3996CQ	650 V	7	14	20	–
900 V PowiGaN Switch		30 VDC	60 VDC	400 VDC	800 VDC
INN3997CQ	650 V	10	20	55	–
INN3999CQ	650 V	10	30	85	–
INN3990CQ	650 V	10	40	100	–
1700 V SiC Switch		30 VDC	60 VDC	400 VDC	800 VDC
INN3947CQ	1200 V	10	23	50	50
INN3949CQ	1200 V	10	40	120	120
INN3947FQ[3]	1200 V	10	23	50	50
INN3949FQ[3]	1200 V	10	40	120	120

Table 1. Output Power Table.

Notes:
1. Maximum output power is dependent on the design. Power delivery is calculated assuming that package temperature must be < 125 °C and that the design uses suitable thermal strategies (e.g. PCB copper area and/or a thermal interface to enclosure).
2. Packages: InSOP-24D and InSOP-T28G.
3. Contact PI for information on UL, TUV, CQC, VDE and DIN EN IEC 60747-17 approvals.

This Product is Covered by Patents and/or Pending Patent Applications.

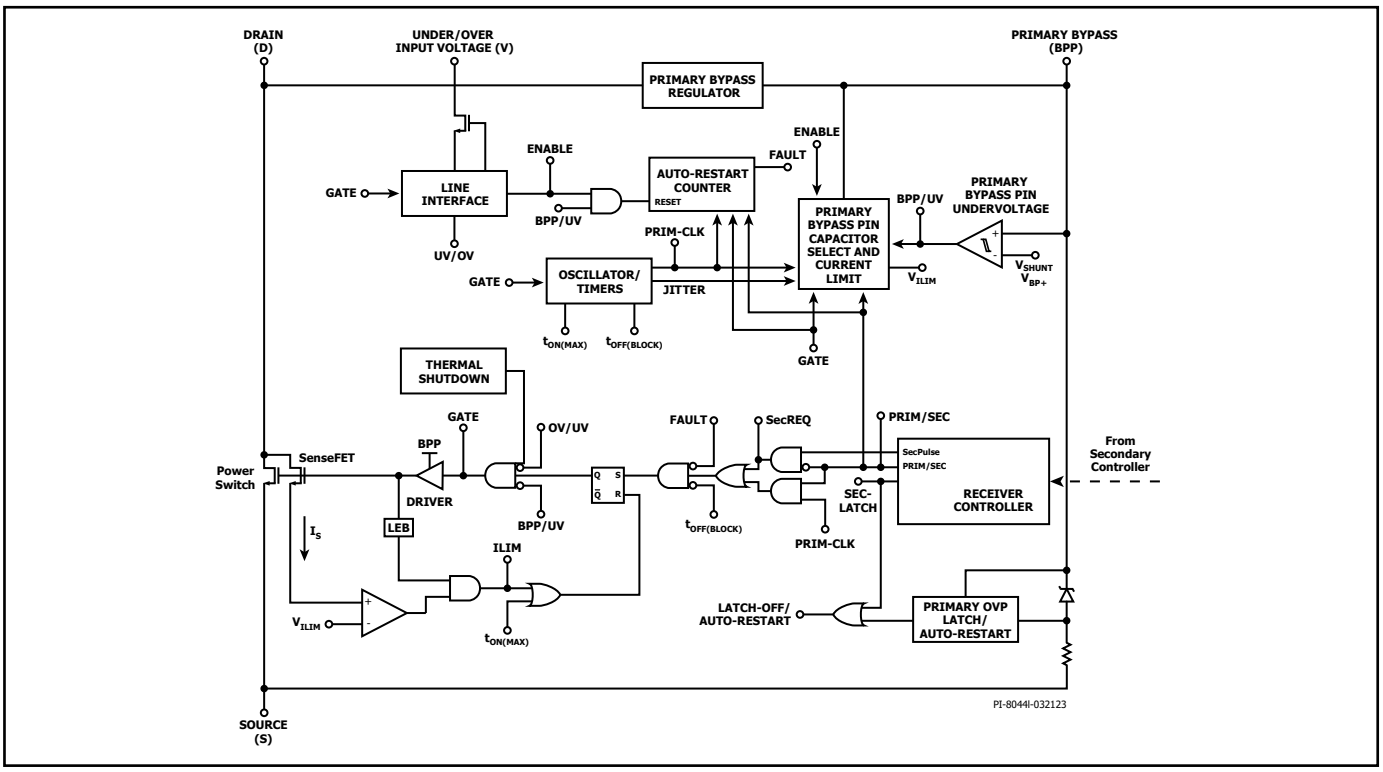


Figure 3. Primary Controller Block Diagram.

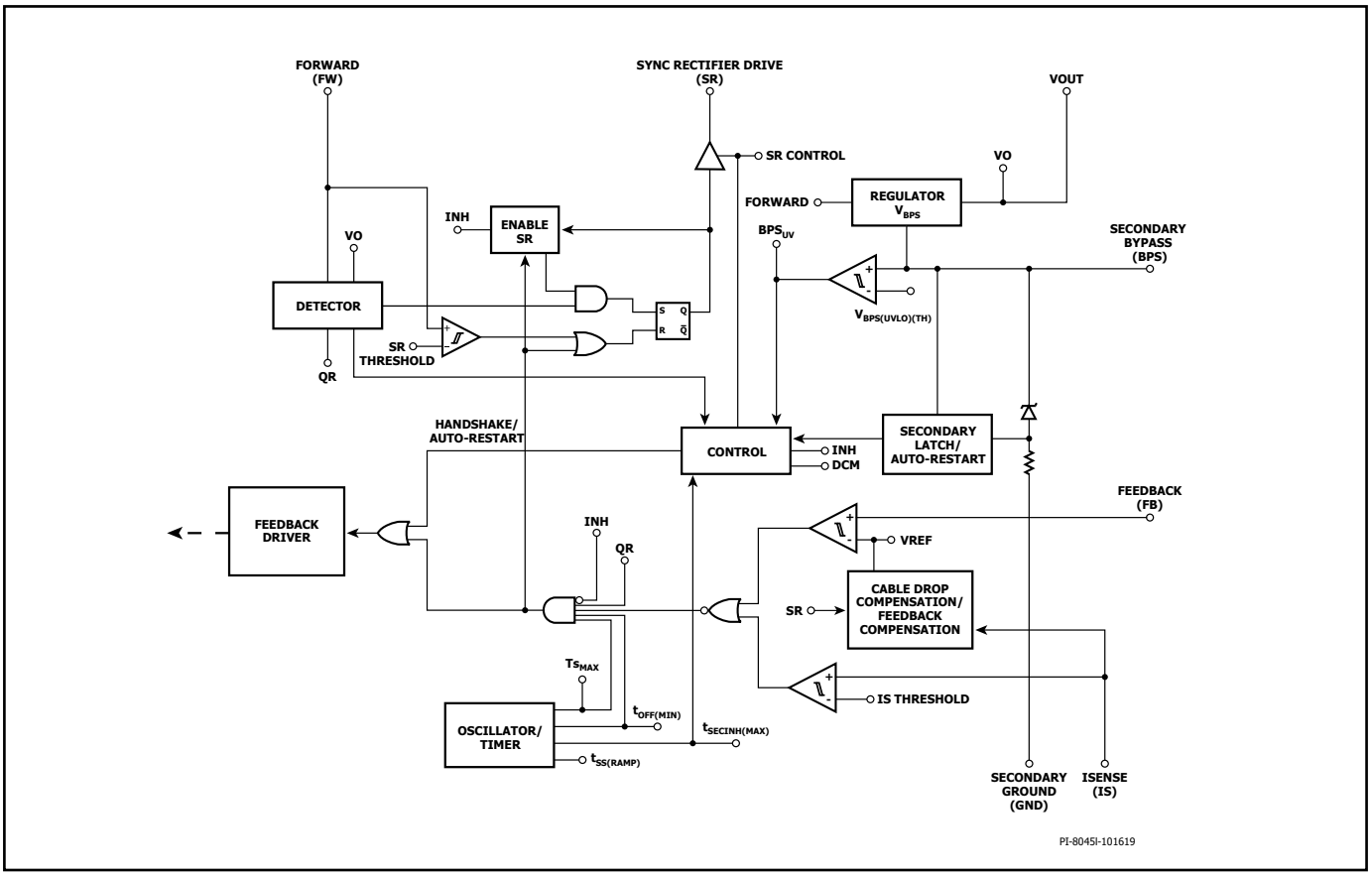


Figure 4. Secondary Controller Block Diagram.

Pin Functional Description – C Package

Secondary-Side Pins

ISENSE (IS) Pin (Pin 1)
Connection to the power supply output terminals. An external current sense resistor should be connected between this and the GND pin. If current regulation/accurate over-current protection is not required, this pin should be tied to the GND pin.

SECONDARY GROUND (GND) (Pin 2)
Ground for the secondary IC. Note this is not the power supply output ground due to the presence of the sense resistor between this and the ISENSE pin.

FEEDBACK (FB) Pin (Pin 3)
Connection to an external resistor divider to set the power supply output voltage.

SECONDARY BYPASS (BPS) Pin (Pin 4)
Connection point for an external bypass capacitor for the secondary IC supply.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 5)
Gate driver for external SR FET. If no SR FET is used connect this pin to GND.

OUTPUT VOLTAGE (VOUT) Pin (Pin 6)
Connected directly to the output voltage, to provide current for the controller on the secondary-side and provide secondary protection.

FORWARD (FWD) Pin (Pin 7)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller when VOUT is below threshold.

NC Pins (Pin 8-12)
Leave open. Should not be connected to any other pins.

Primary-Side Pins

INPUT UNDER/OVERVOLTAGE (V) Pin (Pin 13)
A high-voltage pin for input voltage sensing. One or two current thresholds are provided (depending on device) to provide line undervoltage only or line undervoltage and line overvoltage. These same thresholds can be used to provide remote on/off.

If input voltage sensing is not required, then connect the V pin to SOURCE close to the IC package.

Device	UV	OV	$V_{V(MAX)}$
INN3977CQ	Y	Y	650
INN3996CQ	Y	Y	650
INN3997CQ/INN3999CQ/ INN3990CQ	Y	Y	650[1]
INN3947CQ/INN3949CQ	Y	N	650

Note 1: Applicable before and at start-up. (BYPASS pin < VBPP).

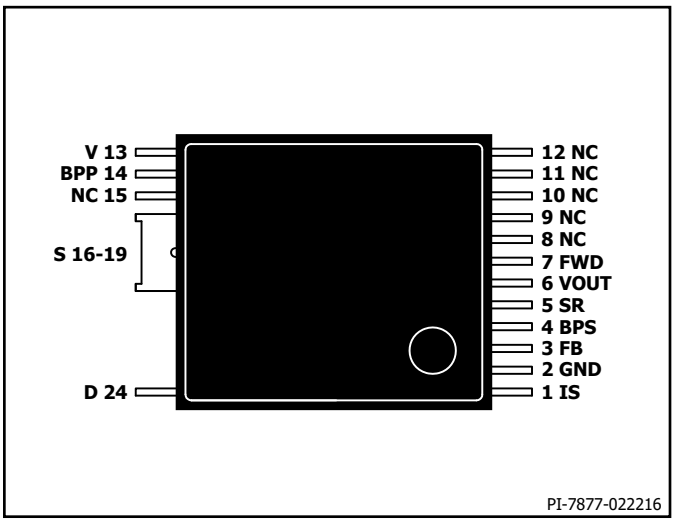


Figure 5. Pin Configuration for C Package.

INN3977CQ/INN3996CQ/INN3947CQ/INN3949CQ
To reduce light and no-load power consumption the V pin is floated when the device switching frequency drops below ~20 kHz. With the pin floated the voltage on the V pin rises to the input voltage and the current through the sense resistor and associated loss reduces to zero. When switching <20 kHz, prior to each switching cycle the pin is pulled to SOURCE and the current is sampled to determine if an UV or OV condition exists. When switching >20 kHz the V pin is held low and the voltage is continuously sensed.

If the maximum input voltage can exceed $V_{V(BVDSS)}$ then the circuit shown in Figure 14 shall be used. This disables the OV feature (INN3977CQ) while leaving UV active and clamps the V pin to ~9 V. More details are provided in application note AN-106.

INN3997CQ/INN3999CQ/INN3990CQ
The INN3997CQ, INN3999CQ and INN3990CQ devices do not have the sampled V pin behavior after start-up. Once the BPP pin voltage reaches V_{BPP} the V pin voltage is clampled to ~1.5 V. Therefore if the V pin voltage at start-up does not exceed $V_{V(BVDSS)}$ then there is no requirement for an external clamping circuit.

PRIMARY BYPASS (BPP) Pin (Pin 14)
The connection point for an external bypass capacitor for the primary-side supply. This is also the ILIM selection pin for choosing standard I_{LIMIT} or $I_{LIMIT+1}$.

NC Pin (Pin 15)
This pin must be left open and not tied to other pins.

SOURCE (S) Pin (Pin 16-19)
These pins are the power switch source and thermal connection. Also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
Power switch drain connection.

Pin Functional Description – F Package

Secondary-Side Pins

ISENSE (IS) Pin (Pin 1)
Connection to the power supply output terminals. An external current sense resistor should be connected between this and the GND pin. If current regulation/accurate over-current protection is not required, this pin should be tied to the GND pin.

SECONDARY GROUND (GND) (Pin 2)
Ground for the secondary IC. Note this is not the power supply output ground due to the presence of the sense resistor between this and the ISENSE pin.

FEEDBACK (FB) Pin (Pin 3)
Connection to an external resistor divider to set the power supply output voltage.

SECONDARY BYPASS (BPS) Pin (Pin 4)
Connection point for an external bypass capacitor for the secondary IC supply.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 5)
Gate driver for external SR FET. If no SR FET is used connect this pin to GND.

OUTPUT VOLTAGE (VOUT) Pin (Pin 7)
Connected directly to the output voltage, to provide current for the controller on the secondary-side and provide secondary protection.

FORWARD (FWD) Pin (Pin 10)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller when VOUT is below threshold.

NC Pins (Pin 6, 8-9, 11-14)
Leave open. Should not be connected to any other pins.

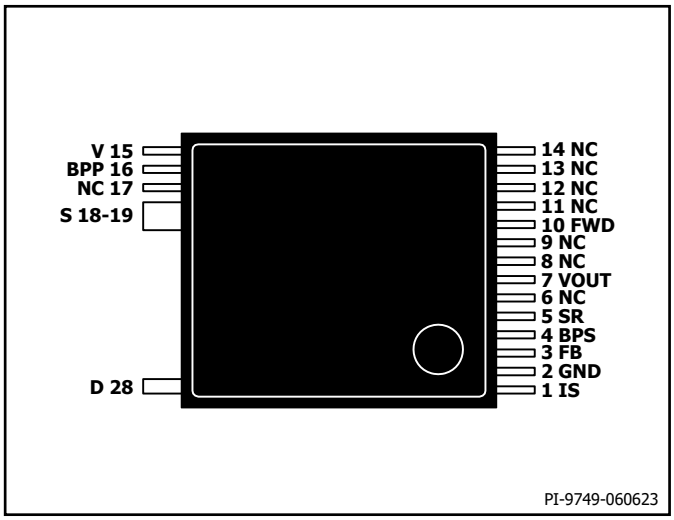


Figure 6. Pin Configuration for F Package.

Primary-Side Pins

INPUT UNDERVOLTAGE & REMOTE CONTROL (V) Pin (Pin 15) INN3947FQ/INN3949FQ
A low voltage pin used to trigger line undervoltage and remote enable/disable through current thresholds. If the pin's maximum input voltage can exceed $V_{V(BVDSS)}$ (650 V) then the circuit shown in Figure 15 shall be used.

PRIMARY BYPASS (BPP) Pin (Pin 16)
The connection point for an external bypass capacitor for the primary-side supply. This is also the ILIM selection pin for choosing standard I_{LIMIT} or $I_{LIMIT+1}$.

NC Pin (Pin 17)
This pin must be left open and not tied to other pins.

SOURCE (S) Pin (Pin 18-19)
These pins are the power switch source and thermal connection. Also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 28)
Power switch drain connection.

InnoSwitch3-AQ Functional Description

The InnoSwitch3-AQ combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme (FluxLink) using the package lead frame and bond wires to provide a safe, reliable, and cost-effective means to transmit accurate, output voltage and current information from the secondary controller to the primary controller.

The primary controller on InnoSwitch3-AQ is a valley switching (DCM) flyback controller that has the ability to operate in continuous conduction mode (CCM), boundary mode (CrM) and discontinuous conduction mode (DCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator, a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, current limit selection circuitry, over-temperature protection, leading edge blanking and a 750 V, 900 V and 1700 V power switch.

The InnoSwitch3-AQ secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, a constant voltage (CV) and a constant current (CC) control circuit, a 4.4 V regulator on the SECONDARY BYPASS pin, QR mode circuit, oscillator and timing circuit, and numerous integrated protection features.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller, highlighting the most important features.

Primary Controller

InnoSwitch3-AQ has variable frequency valley switching controller plus CCM/CrM/DCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power MOSFET is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power MOSFET is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch3-AQ to be powered externally through a bias winding, decreasing the no-load consumption to less than 15 mW.

Primary Bypass I_{LIMIT} Programming

InnoSwitch3-AQ ICs allows the user to adjust current limit (I_{LIMIT}) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor should be used.

There are 2 selectable capacitor sizes - 0.47 µF and 4.7 µF for setting standard and increased I_{LIMIT} settings respectively.

Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power MOSFET when the PRIMARY BYPASS pin voltage drops below ~4.5 V ($V_{BPP} - V_{BPP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to V_{SHUNT} to re-enable turn-on of the power MOSFET.

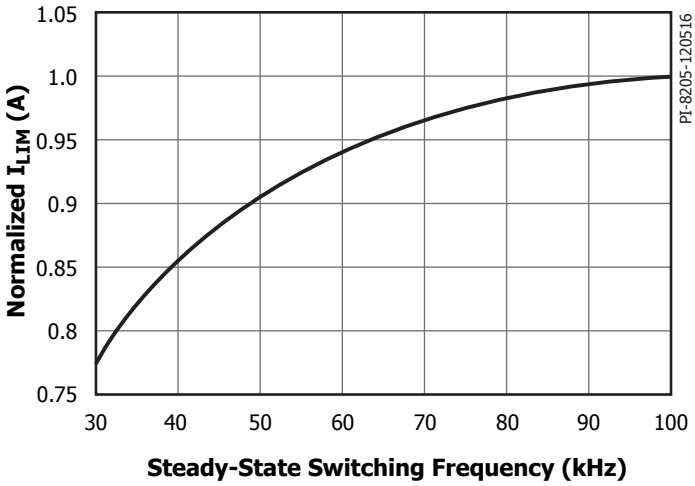


Figure 7. Normalized Primary Current vs. Frequency.

Primary Bypass Output Overvoltage Function

The PRIMARY BYPASS pin has an OV protection feature. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds I_{SD}, the device will disable the power MOSFET switching for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation.

Output overvoltage protection is also included as an integrated feature on the secondary controller (see Output Voltage Protection).

Over-Temperature Protection

The thermal shutdown circuitry senses the primary MOSFET die temperature. The threshold is set to T_{SD} with a hysteretic response.

If the die temperature rises above the threshold, the power MOSFET is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent overheating of the PCB due to a continuous fault condition.

Current Limit Operation

The primary-side controller has a current limit threshold ramp that is linearly decreased during the time from the end of the previous primary switching cycle (i.e. from the time the primary MOSFET turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 7).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current approaching 100% I_{LIMIT}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase (lowering frequency) as load reduces.

Note the controller provides excellent transient load response, being able to slow to full frequency, current and therefore output power within one switching cycle.

Jitter
To reduce EMI the normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M. This results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart
In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch3-AQ enters auto-restart (AR).

In auto-restart, switching of the power MOSFET is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency f_{OVL} (~110 kHz) for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for >$t_{AR(SK)}$.

   The secondary will stop sending requests under two fault cases:

   a. No response detection to 8 consecutive secondary requests.
   b. 4 consecutive unrequested switching detections.

The second is included to ensure that if communication is lost, the primary tries to restart. Although this should never be the case in normal operation. The issue is resolved when the primary restarts after an auto-restart off-time.

SOA Protection
In the event that there are two consecutive cycles where the 1.1 × I_{LIM} is reached within ~565 ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or ~25 µs (based on full frequency of 100 kHz). This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

Remote Enable/Disable Function
INN3997CQ/INN3999CQ/INN3990CQ/INN3947FQ/ INN3949FQ
InnoSwitch3-AQ has a remote-control function allowing for external enabling and disabling of device operation through its V pin. When current sinking into V pin exceeds I_{OV+}, the InnoSwitch3-AQ is disabled and goes into standby mode. In standby mode the InnoSwitch3-AQ does not switch. To enable, lower the V pin current below I_{OV-}.

Primary-Secondary Handshake
At start-up, the primary-side initially switches without any feedback information.

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from the OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

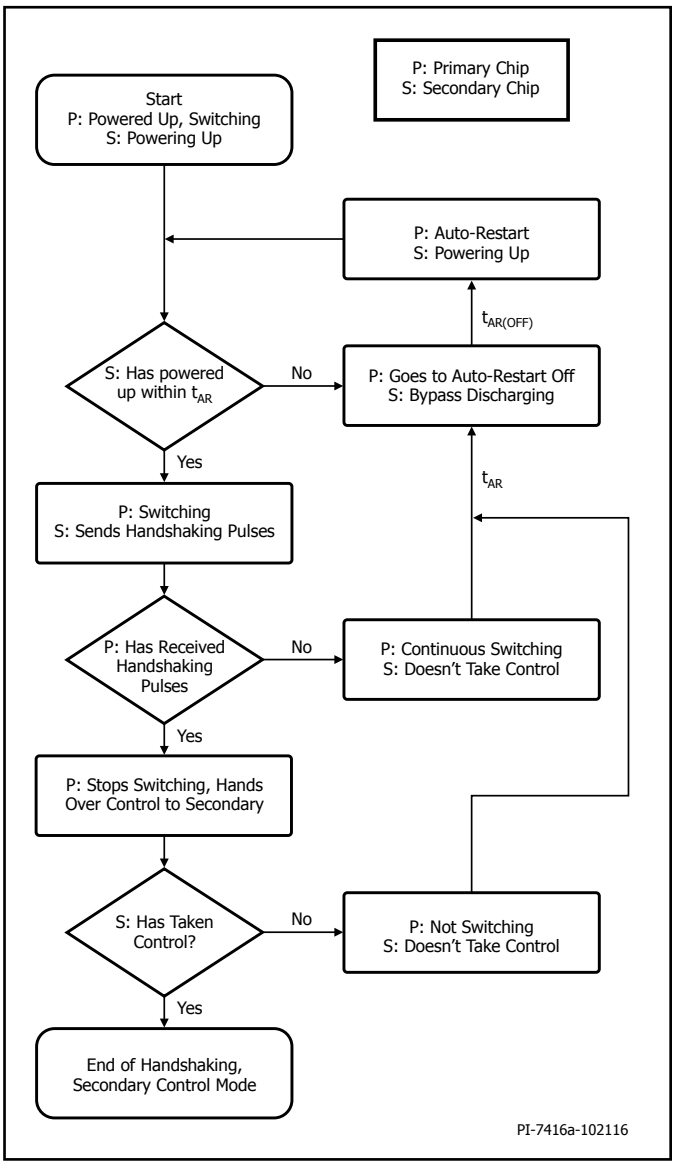


Figure 8. Primary-Secondary Handshake Flowchart.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary DC-link brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If the secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen
When the primary resumes switching after initial power-up recovery from an DC-link voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller (follows operation).

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in response to secondary requests. If no pulses occurs during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine
The InnoSwitch3-AQ features an active audible noise reduction mode whereby the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 7 kHz and 12 kHz - 143 µs and 83 µs. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power MOSFET is inhibited.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered by a 4.4 V (V_{BPS}) regulator which is supplied by either VOUT or FWD. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing.

The mid-point of an external resistor divider network between the OUTPUT VOLTAGE and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate the output voltage. The internal voltage comparator reference voltage is V_{FB} (1.265 V).

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins is used to regulate the output current in constant current regulation mode.

Minimum Off-Time
The secondary controller initiates a cycle request using the inductive-connection to the primary. The maximum frequency of secondary-cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency
The maximum switch-request frequency of the secondary controller is f_{SREQ}.

Frequency Soft-Start
At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

The secondary controller temporarily inhibits the FEEDBACK short protection threshold ($V_{FB(OFF)}$) until the end of the soft-start ($t_{SS(RAMP)}$) time. After hand-shake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the $t_{SS(RAMP)}$ time period.

In the event of a short-circuit or overload at start-up, the device will move directly into CC (constant-current) mode. The device will go into auto-restart (AR), if the output voltage does not rise above the $V_{FB(AR)}$ threshold before the expiration of the ($t_{FB(AR)}$) timer after handshake has occurred.

The secondary controller enables the FEEDBACK pin-short protection mode ($V_{FB(OFF)}$) at the end of the $t_{FB(AR)}$ time period. If the output short maintains the FEEDBACK pin below the short-circuit threshold, the secondary will stop requesting pulses triggering an auto-restart cycle.

If the output voltage reaches regulation within the $t_{SS(RAMP)}$ time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant-detection has already occurred.

Maximum Secondary Inhibit Period
Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30 µs.

Output Voltage Protection
In the event that the sensed voltage on the FEEDBACK pin is 2% higher than the regulation threshold, a bleed current of ~2.5 mA (3 mA max) is applied on the OUTPUT VOLTAGE pin (weak bleed). This bleed current increases to ~200 mA (strong bleed) in the event that the FEEDBACK pin voltage is raised beyond ~10% of the internal FEEDBACK pin reference voltage. The current sink on the OUTPUT VOLTAGE pin is intended to discharge the output voltage after momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

If the voltage on the FEEDBACK pin is sensed to be 20% higher than the regulation threshold, a command is sent to the primary to begin an auto-restart sequence. This integrated V_{OUT} OVP can be used independently from the primary sensed OVP or in conjunction.

FEEDBACK Pin Short Detection
If the sensed FEEDBACK pin voltage is below $V_{FB(OFF)}$ at start-up, the secondary controller will complete the handshake to take control of the primary complete $t_{SS(RAMP)}$ and will stop requesting cycles to initiate auto-restart (no cycle requests made to primary for longer than $t_{AR(SK)}$ second triggers auto-restart).

During normal operation, the secondary will stop requesting pulses from the primary to initiate an auto-restart cycle when the FEEDBACK pin voltage falls below the $V_{FB(OFF)}$ threshold. The deglitch filter on the protection mode is on for less than ~10 µs. By this mechanism, the secondary will relinquish control after detecting that the FEEDBACK pin is shorted to ground.

Auto-Restart Thresholds
The OUTPUT VOLTAGE pin includes a comparator to detect when the output voltage falls below $V_{FB(AR)}$, for a duration exceeding $t_{FB(AR)}$ respectively. The secondary controller will relinquish control when this fault condition is detected. This threshold is meant to limit the range of constant current (CC) operation.

SECONDARY BYPASS Pin Overvoltage Protection
The InnoSwitch3-AQ secondary controller features a SECONDARY BYPASS pin OV feature similar to the PRIMARY BYPASS pin OV feature. When the secondary is in control, in the event that the SECONDARY BYPASS pin current exceeds $I_{BPS(SD)}$ (~9 mA) the secondary will send a command to the primary to initiate an auto-restart off-time ($t_{AR(OFF)}$).

Output Constant Current
The InnoSwitch3-AQ regulates the output current through an external current sense resistor between the ISENSE and SECONDARY GROUND pins. If constant current regulation/output current limitation is not required, the ISENSE pin must be tied to the SECONDARY GROUND pin.

Intelligent Valley Switching Mode
In order to improve conversion efficiency and reduce switching losses, the InnoSwitch3-AQ features a means to force switching when the voltage across the primary switch is near its minimum when the converter operates in discontinuous conduction mode (DCM). This mode of operation is automatically engaged in DCM and disabled once the converter moves to continuous-conduction mode (CCM).

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power MOSFET.

Valley switching (VS) mode is enabled for 20 μs after DCM is detected or when ring amplitude (pk-pk) >2 V. Afterwards, VS switching is disabled, at which point switching may occur at any time a secondary request is initiated.

The secondary controller includes blanking of ~1 μs to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground. See Figure 9.

SR Disable Protection
In each cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event that the voltage on the ISENSE pin exceeds approximately 3 times the CC threshold, the SR FET drive is disabled until the surge current has diminished to nominal levels.

SR Static Pull-Down
To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has a nominally "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection
In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 100 pF, the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above 100 pF, the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCH-RONOUS RECTIFIER DRIVE pin protection mode is also disabled.

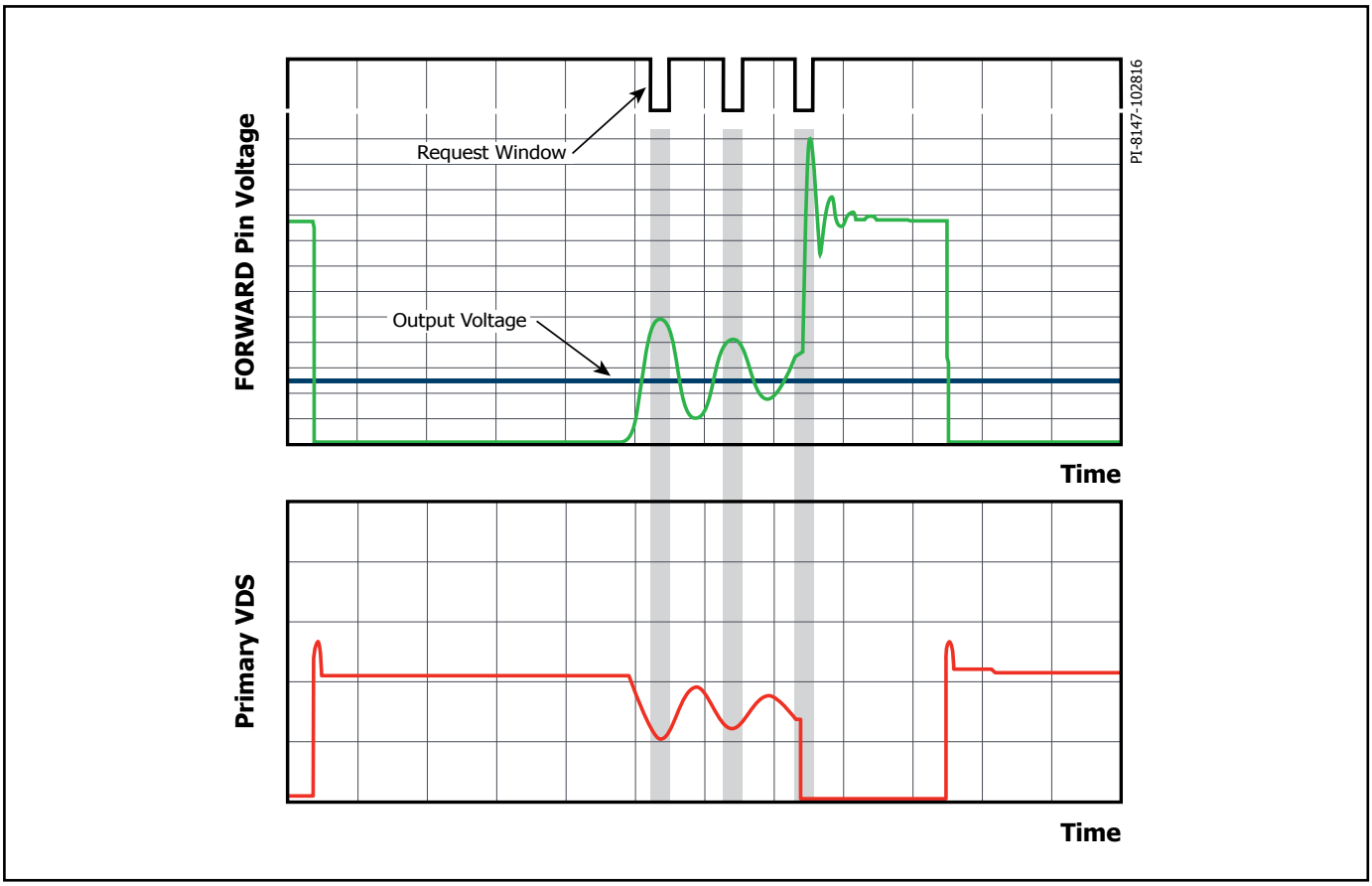


Figure 9. Intelligent Quasi-Resonant Mode Switching.

Applications Example

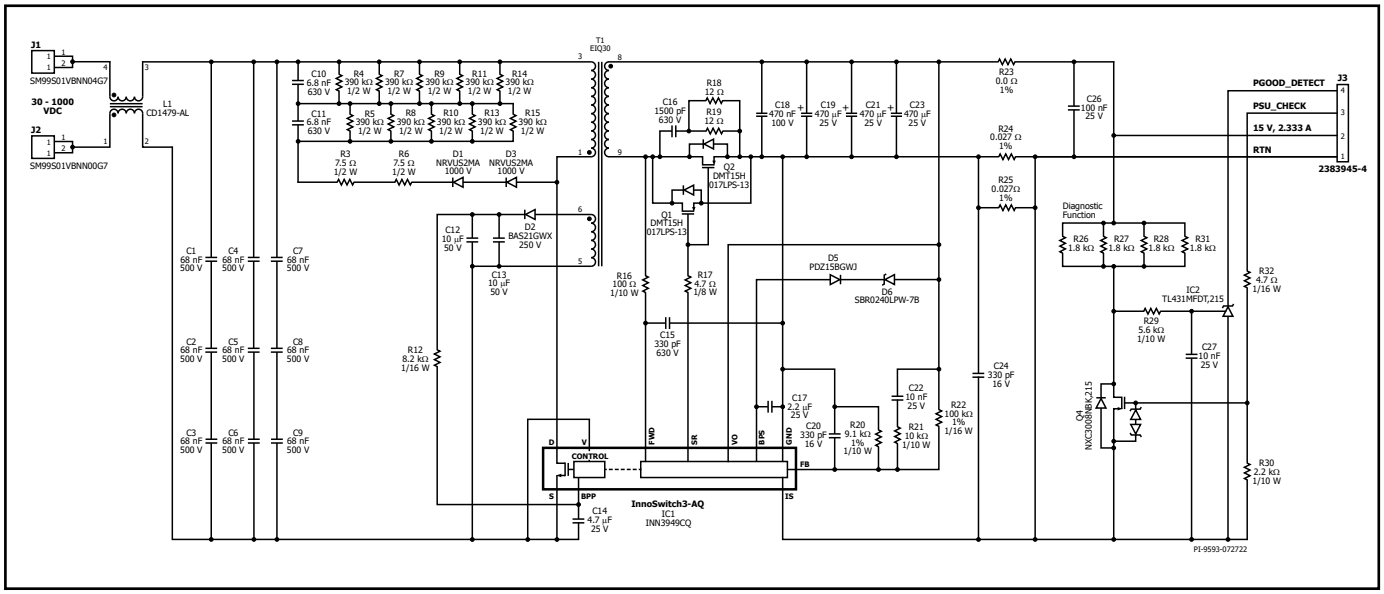


Figure 10. 12 V, 30 W Power Supply.

Primary-Side

The circuit shown in Figure 10 is a reinforced isolated wide input voltage 15 V, 35 W power supply using INN3949CQ. This is a typical example of an emergency power supply for traction inverters.

The input is filtered by an optional common mode choke (L1). This is included to reduce common currents flowing from the DC output to the DC input created by the traction inverter operation.

Local DC input decoupling is provided by C1 to C9, multiple components are used in series to avoid a single point failure shorting the DC input, voltage derating, reduce the creepage distance needed at PCB pads and ease sourcing as lower voltage capacitors are generally more available.

Similar reasoning is used for the components in the primary clamp network, including multiple resistors in parallel to meet power derating.

One end of the transformer primary is connected to the DC bus; the other is connected to the integrated power switch the InnoSwitch3-AQ IC (U1). A low cost RCD clamp formed by D1, D3, R3-R14, C10 and C11 limits the peak drain voltage of U1 at the instant of turn-off of the internal switch due to leakage inductance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C14) when DC input voltage is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C13. Resistor R12 limits the current being supplied to the BPP pin of InnoSwitch3-AQ IC (U1).

Secondary-Side

The secondary-side of the INN3949CQ IC provides output voltage, output current sensing, and drive to MOSFETs providing synchronous rectification (SR). A RC network formed by R18, R19 and C16 damps high frequency ringing across SR FETs Q1 and Q2, which results from leakage inductance of the transformer windings and the secondary trace inductances. The rectified output is filtered by Low ESR polymer capacitors, C18, C19, C21, C23. Resistor R23 is a provision to allow an inductor to be added to further reduce output ripple if required.

The gates of Q1 and Q2 are turned on based on the winding voltage sensed via R16 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin, charging the decoupling capacitor C17 via an internal regulator. Resistors R20 and R22 form a voltage divider network that senses the output voltage, compared to the 1.265 V reference level on the FB pin. Capacitor C20 provides decoupling from high frequency noise affecting power supply operation, C22 and R21 form a feed forward network to increase response time to lower the output ripple. The output current is sensed by R24 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across this resistor is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.

The design includes two diagnostic functions. The PSU_CHECK input allows a small load (R26,27,28,31) to be enabled. The PGOOD_ DETECT is an active low output that indicates the output is present (>2.5 V). When the output of this supply is diode OR'd to another supply for redundancy the PSU_CHECK input allows the system to determine that the supply is operating correctly by monitoring the output voltage before the ORing diode.

Key Application Considerations

Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following conditions:

1. The minimum DC input voltage as shown.
2. Efficiency assumptions depend on power level. The power level assumes efficiency > 89 %.
3. Transformer primary inductance tolerance of ±10%.
4. Maximum conduction losses is limited to 0.8 W.
5. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 125 °C.
6. Below a value of 1, K_p is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_p limit of ≥0.25 is recommended. This prevents the turn-on edge current spike from triggering the current limit.

Primary-Side Overvoltage Protection

Primary-side output overvoltage protection provided by the InnoSwitch3-AQ IC's is triggered by a threshold current of I_{SD} into the PRIMARY BYPASS pin. In addition to an internal filter, the PRIMARY BYPASS pin capacitor forms an external filter helping noise immunity. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

The primary sensed OVP function can be realized by connecting a series combination of a Zener diode, a resistor and a blocking diode from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin. The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) due to poor coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. This measurement should be ideally done at the lowest input voltage and with highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. It is recommended that a Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered be selected. A forward voltage drop of 1 V can be assumed for the blocking diode. A small signal standard recovery diode is recommended. The blocking diode prevents any reverse current discharging the bias capacitor during start-up. Finally, the value of the series resistor required can be calculated such that a current higher than I_{SD} will flow into the PRIMARY BYPASS pin during an output overvoltage.

Reducing No-Load Consumption

The InnoSwitch3-AQ IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. Use of a bias winding is however required to provide supply current to the PRIMARY BYPASS pin once the InnoSwitch3-AQ IC has started switching. An auxiliary (bias) winding provided on the transformer serves this purpose. A bias winding driver supply to the PRIMARY BYPASS pin enables design of power supplies with no-load power consumption less than 15 mW. Resistor R4 shown in Figure 10 should be adjusted to achieve the lowest no-load input power.

Secondary-Side Overvoltage Protection (Auto-Restart Mode)

The secondary-side output overvoltage protection provided by the InnoSwitch3-AQ IC uses an internal auto restart circuit that is triggered by an input current exceeding a threshold of $I_{BPS(SD)}$ into the SECONDARY BYPASS pin. The direct output sensed OVP function can be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage needs to be the difference between 1.25 × V_{OUT} and 4.4 V the SECONDARY BYPASS pin voltage. It is necessary to add a low value resistor in series with the OVP Zener diode to limit the maximum current into the SECONDARY BYPASS pin.

Selection of Components

Components for InnoSwitch3-AQ Primary-Side Circuit

BPP Capacitor

A capacitor connected from the PRIMARY BYPASS pin of the InnoSwitch3-AQ IC to GND provides decoupling for the primary-side controller and also selects current limit. A 0.47 µF or 4.7 µF capacitor may be used. Multi-layer ceramic capacitors are preferred they enable placement of capacitors close to the IC and meet automotive temperature requirements. At least 10 V, 0805 or larger size rated X7R dielectric capacitors are recommended to ensure that minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

INN3997CQ/INN3999CQ/INN3947CQ/INN3949CQ

To prevent IC damage in the event the BP capacitor fails open circuit it is recommended to place an additional 100 nF capacitor in parallel to the 0.47 µF or 4.7 µF capacitor selected.

Bias Winding and External Bias Circuit

The internal regulator connected from the DRAIN pin of the switch to the PRIMARY BYPASS pin of the InnoSwitch3-AQ primary-side controller charges the capacitor connected to the PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply at least 1 mA of current to the PRIMARY BYPASS pin. The turns ratio for the bias winding should be selected such that 7 V is developed across the bias winding at the lowest rated output voltage of the power supply at the lowest load condition. If the voltage is lower than this, no-load input power will increase.

The bias current from the external circuit should be set to approximately $I_{S1(MAX)}$ to achieve lowest no-load power consumption when operating the power supply at the highest DC input voltage, (V_{BPP} > 5 V). A standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes. A ceramic capacitor of at least 22 µF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended (C3 in Figure 10). Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and load with the lowest input DC supply voltage.

Primary Sensed OVP (Overvoltage Protection)
The voltage developed across the output of the bias winding tracks the power supply output voltage. Though not precise, a reasonable detection of the amplitude of the output voltage can be achieved by the primary-side controller using the bias winding voltage. A Zener diode connected from the bias winding output to the PRIMARY BYPASS pin can reliably detect a secondary overvoltage fault and cause the primary-side controller to auto-restart. It is recommended that the highest voltage at the output of the bias winding should be measured for normal steady- state conditions (at full load and lowest input voltage) and also under transient load conditions. A Zener diode rated for 1.25 times this measured voltage will typically ensure that OVP protection will only operate in case of a fault.

Primary-Side Snubber Clamp
A snubber circuit should be used on the primary-side as shown in Figure 10. This prevents excess voltage spikes at the drain of the switch at the instant of turn-off of the switch during each switching cycle. Though conventional RCD clamps can be used, RCDZ clamps offer the highest efficiency. The circuit example shown in Figure 10 uses an RCD clamp with a resistor in series with the clamp diode. This resistor dampens the ringing at the drain and also limits the reverse current through the clamp diode during reverse recovery. Standard recovery glass passivated diodes with low junction capacitance are recommended as these enable partial energy recovery from the clamp thereby improving efficiency.

Components for InnoSwitch3-AQ Secondary-Side Circuit

SECONDARY BYPASS Pin – Decoupling Capacitor
A 2.2 uF, 10 V / X7R / 0805 or larger size multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch3-AQ IC. Since the SECONDARY BYPASS Pin voltage needs to be 4.4 V before the output voltage reaches the regulation voltage level, a significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. Values lower than 1.5 μF can cause unpredictable operation. The capacitor must be located adjacent to the IC pins. At least 10 V voltage rating is recommended to give enough margin from BPS voltage, and 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCC is not recommended for this reason. The ceramic capacitor type designations, such as X7R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.4 V. Capacitors with X7R dielectrics should be used for best results.

FORWARD Pin Resistor
A resistor in the range of 47 Ω to 100 Ω resistor is recommended to ensure sufficient IC supply current. A higher or lower resistor value should not be used as it can affect device operation such as the timing of the synchronous rectifier drive. Figures 11, 12, 13, and 14 below show examples of unacceptable and acceptable FORWARD pin voltage waveforms. V_D is forward voltage drop across the SR.

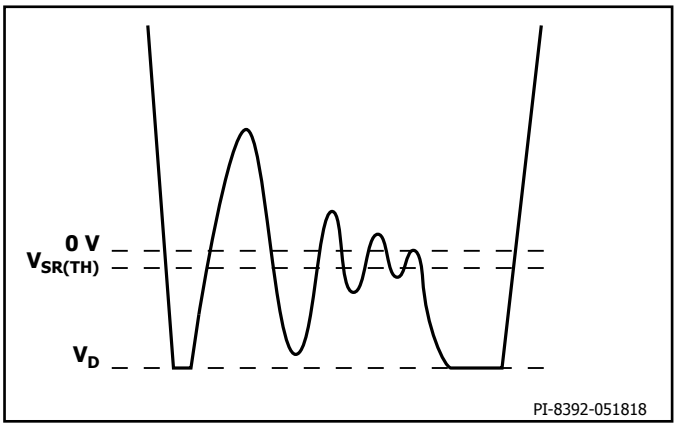


Figure 11. Unacceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

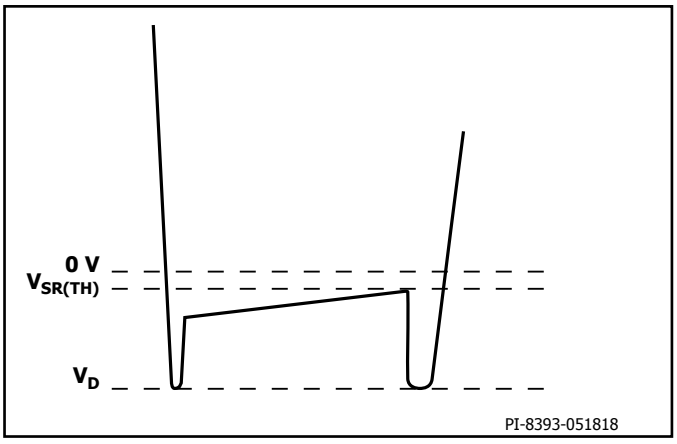


Figure 12. Acceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

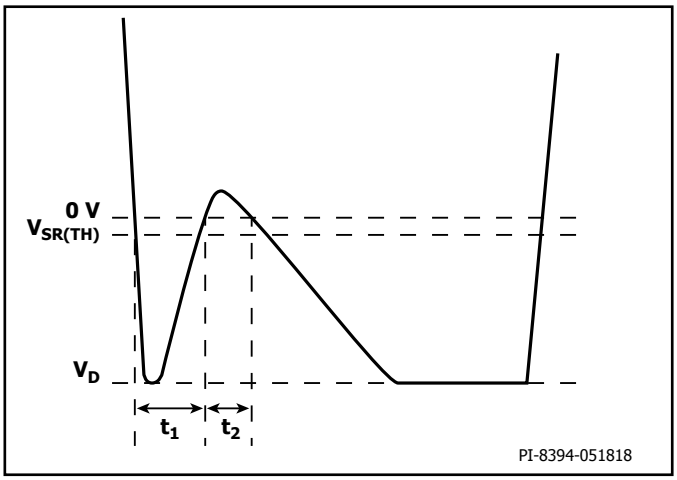


Figure 13. Unacceptable FORWARD Pin Waveform before Handshake with Body Diode Conduction During Flyback Cycle.

Note:
If $t_1 + t_2 = 1.5\ \mu s \pm 50$ ns, the controller may fail the handshake and trigger a primary bias winding OVP latch-off/auto-restart.

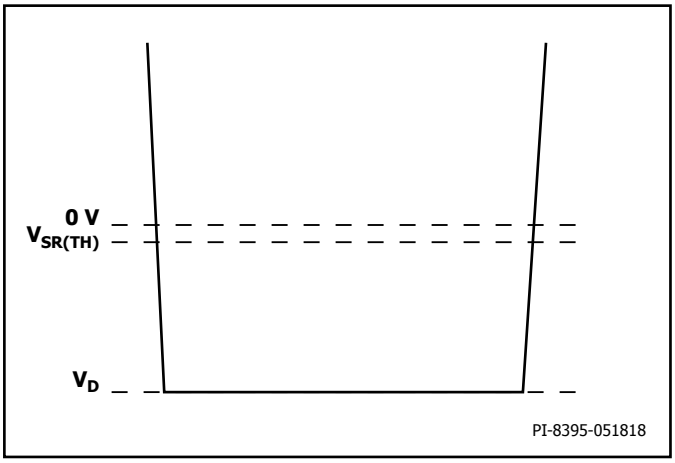


Figure 14. Acceptable FORWARD Pin Waveform before Handshake with Body Diode Conduction During Flyback Cycle.

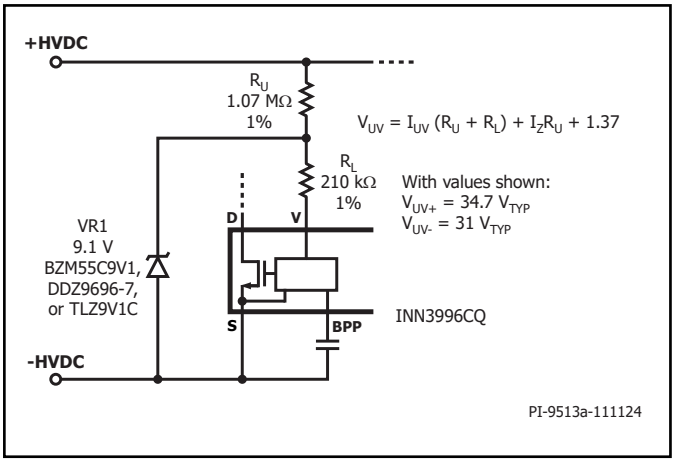


Figure 15. Circuit to Enable UV, Disable OV and Clamp V Pin Below Maximum Voltage Rating.

SR Switch Operation and Selection

Although a simple diode rectifier and filter works for the output, use of an SR FET enables significant improvement in operating efficiency and reduction in loss and component cost compared to large Schottky rectifiers. The secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch3-AQ IC (no additional resistors should be connected in the gate circuit of the SR FET). The SR FET is turned off once the voltage V_{DS} of SR FET reaches 0 V. The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.4 V. A FET with a high threshold voltage is therefore not suitable. FETs with a threshold voltage of 1.5 V to 2.5 V are ideal although switches with a threshold voltage (absolute maximum) as high as 4 V may be used provided their data sheets specify $R_{DS(ON)}$ across temperature for a gate voltage of 4.5 V.

There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the InnoSwitch3-AQ IC detects end of the flyback cycle, voltage across SR FET $R_{DS(ON)}$ reaches 0 V, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET or the external parallel Schottky diode. Use of the Schottky diode parallel to the SR FET may provide higher efficiency and typically a 1 A surface mount Schottky diode is adequate. The voltage rating of the Schottky diode and the SR FET should be at least 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. The interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) leads to ringing on the voltage waveform at the instant of voltage reversal at the winding due to primary switch turn-on. This ringing can be suppressed using an RC snubber connected across the SR FET. A snubber resistor in the range of 10 ohms to 47 ohms may be used (higher resistance values lead to noticeable drop in efficiency). A capacitance value of 1 nF to 2.2 nF is adequate for most designs.

Output Capacitor

Due to automotive operating temperatures below -20 ºC solid polymer types are recommended. In this case 150 µF to 330 µF of capacitance per ampere of output current is adequate. This also typically results in acceptable output ripple (<1%). Ensure that capacitors with a voltage rating higher than the highest output voltage plus sufficient margin be used.

Output Voltage Feedback Circuit

The output voltage FEEDBACK pin voltage is 1.265 V [V_{FB}]. A voltage divider network should be connected at the output of the power supply to divide the output voltage such that the voltage at the FEEDBACK pin will be 1.265 V when the output is at its desired voltage. The lower feedback divider resistor should be tied to the SECONDARY GROUND pin. A 300 pF (or smaller) decoupling capacitor should be connected at the FEEDBACK pin to the SECONDARY GROUND pin of the InnoSwitch3-AQ IC. This capacitor should be placed close to the InnoSwitch3-AQ IC.

Recommendations for Circuit Board Layout

See Figure 16 for a recommended circuit board layout for an InnoSwitch3-AQ based power supply.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors
The PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

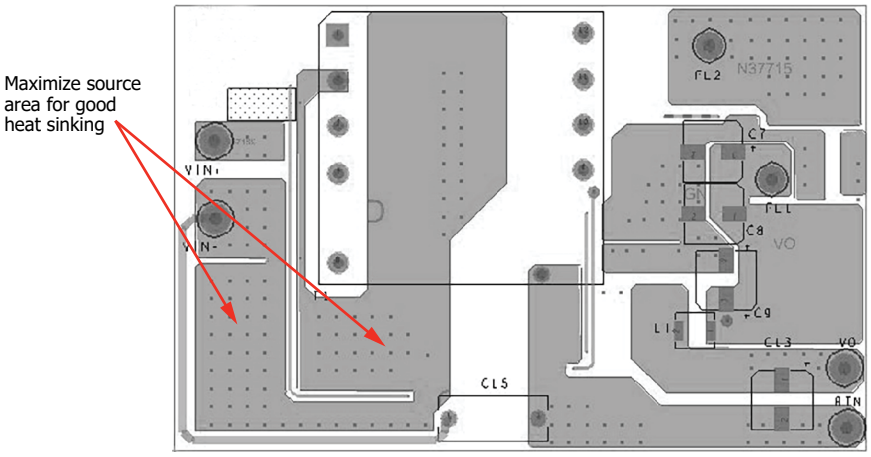
Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and IC.

Thermal Considerations
The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without compromising EMI performance. Similarly for the output SR switch, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR switch. Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 125 °C when operating the power supply at each input voltage condition, corresponding maximum load and ambient temperature. The use of thermal pads between the PCB source area and the enclosure is an effective method to lower device temperature.

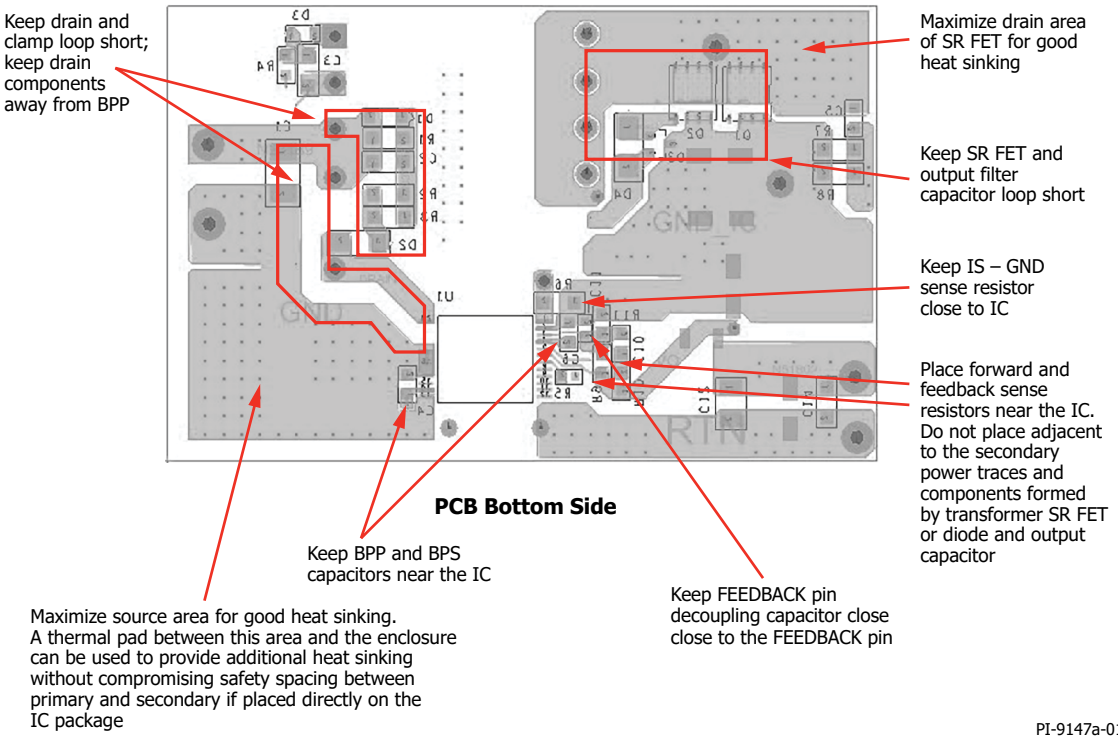
Output SR Switch
For best performance, the area of the loop connecting the secondary winding, the output SR switch and the output filter capacitor, should be minimized.

Drain Node
The drain switching node is the dominant noise generator. As such, the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and trace lengths minimized. The loop area of the loop comprising of the input rectifier filter capacitor, the primary winding and the IC primary-side switch should be kept as small as possible.

Layout Example



PCB Top Side



PCB Bottom Side

Figure 16. PCB Design.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area.
2. A small capacitor in parallel to the clamp diode on the primary-side can help reduce radiated EMI.
3. A resistor in series with the bias winding helps reduce radiated EMI.
4. Adjusting SR switch RC snubber component values can help reduce high frequency radiated and conducted EMI.
5. A pi-filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI
6. A 1 μF ceramic capacitor connected at the output of the power supply helps to reduce radiated EMI.

Recommendations for Transformer Design

Transformer design must ensure that the power supply delivers the rated power at the lowest input voltage. It is recommended that a K_P close to 0.9 at the minimum expected DC bus voltage should be used for most InnoSwitch3-AQ designs. A K_P value of <1 results in higher transformer efficiency by lowering the primary RMS current but results in higher switching losses in the primary-side switch resulting in higher InnoSwitch3-AQ temperature. The benefits of quasi-resonant switching start to diminish for a further reduction of K_P.

Switching Frequency (f_{SW})

It is a unique feature in InnoSwitch3-AQ that for full load, the designer can set the switching frequency to between 25 kHz to 95 kHz. For lowest temperature, the switching frequency should be set to around 60 kHz. For a smaller transformer, the full load switching frequency can be set up to 95 kHz. When setting the full load switching frequency it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed 110 kHz which may trigger auto-restart due to overload protection.

Reflected Output Voltage, V_{OR} (V)

This parameter describes the effect on the primary switch drain voltage of the secondary-winding voltage during diode/SR conduction which is reflected back to the primary through the turns ratio of the transformer. To make full use of QR capability and ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.8 at minimum input voltage and K_P = 1 for high input voltage conditions.

Consider the following for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch3-AQ device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR switches.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.
5. For maximum power delivery at low (30 VDC – 40 VDC) input target the design has to have a primary inductance <500 μH with the lower limit defined by minimum on time of 560 ns at $V_{IN(MAX)}$.

There are some exceptions to this. For output voltages above 15 V, V_{OR} should be higher to maintain an acceptable PIV across the output synchronous rectifier.

Ripple to Peak Current Ratio, K_P

A K_P below 1 indicates continuous conduction mode, where K_P is the ratio of ripple-current to peak-primary-current (Figure 17).

$$K_P = K_{RP} = I_R / I_P$$

A value of K_P higher than 1, indicates discontinuous conduction mode. In this case K_P is the ratio of primary switch off-time to the secondary diode conduction-time.

$$K_P = K_{DP} = (1 - D) \times T/ t = V_{OR} \times (1 - D_{MAX}) / ((V_{MIN} - V_{DS}) \times D_{MAX})$$

It is recommended that a K_P close to 0.9 at the minimum expected DC bus voltage should be used for most InnoSwitch3-AQ designs. A K_P value of <1 results in higher transformer efficiency by lowering the primary RMS current but results in higher switching losses in the primary-side switch resulting in higher InnoSwitch3-AQ temperature. The benefits of quasi-resonant switching start to diminish for a further reduction of K_P. The PIXIs spreadsheet can be used to effectively optimize selection of K_P, inductance of the primary winding, transformer turns ratio, and the operating frequency while ensuring appropriate design margins.

Core Type

Choice of a suitable core is dependent on the physical limits of the power supply enclosure. It is recommended that only cores with low loss be used to reduce thermal challenges.

Safety Margin, M (mm)

Designs that require isolation between primary and secondary may require tape margins on each side of the bobbin. This is especially likely when triple or fully insulated wire types are not used. Refer to the controlling document (specification or standard such as IEC 60664-1) and bobbin data sheet for guidance on margins required to meet creepage distances specified.

It is recommended that for compact transformer designs using an InnoSwitch3-AQ IC, triple insulated or fully insulated wire should be used.

Primary Layers, L

Primary layers should be in the range of 1 ≤ L ≤ 3 and in general should be the lowest number that meets the primary current density limit (CMA). A value of ≥200 cmil / Amp can be used as a starting point for most designs. Higher values may be required due to thermal constraints. Designs with more than 3 layers are possible but the increased leakage inductance and the physical fit of the windings should be considered. A split primary construction may be helpful for designs where clamp dissipation due to leakage inductance is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. This arrangement is often disadvantageous for low power designs as this typically increases common mode noise and adds cost to the input filtering.

Maximum Operating Flux Density, B_M (Gauss)
A maximum value of 3800 gauss at the peak device current limit (at 132 kHz) is recommended to limit the peak flux density at start-up and under output short-circuit conditions. Under these conditions the output voltage is low and little reset of the transformer occurs during the switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch3-AQ IC provide sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

Transformer Primary Inductance, (L_p)
Once the lowest operating input voltage, switching frequency at full load, and required V_{OR} are determined, the transformers primary inductance can be calculated. The PIXIs design spreadsheet can be used to assist in designing the transformer.

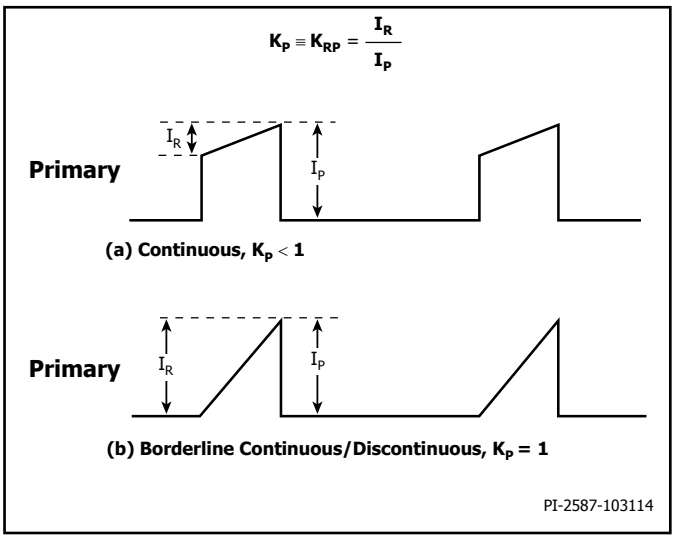


Figure 17. Continuous Conduction Mode Current Waveform, $K_p < 1$.

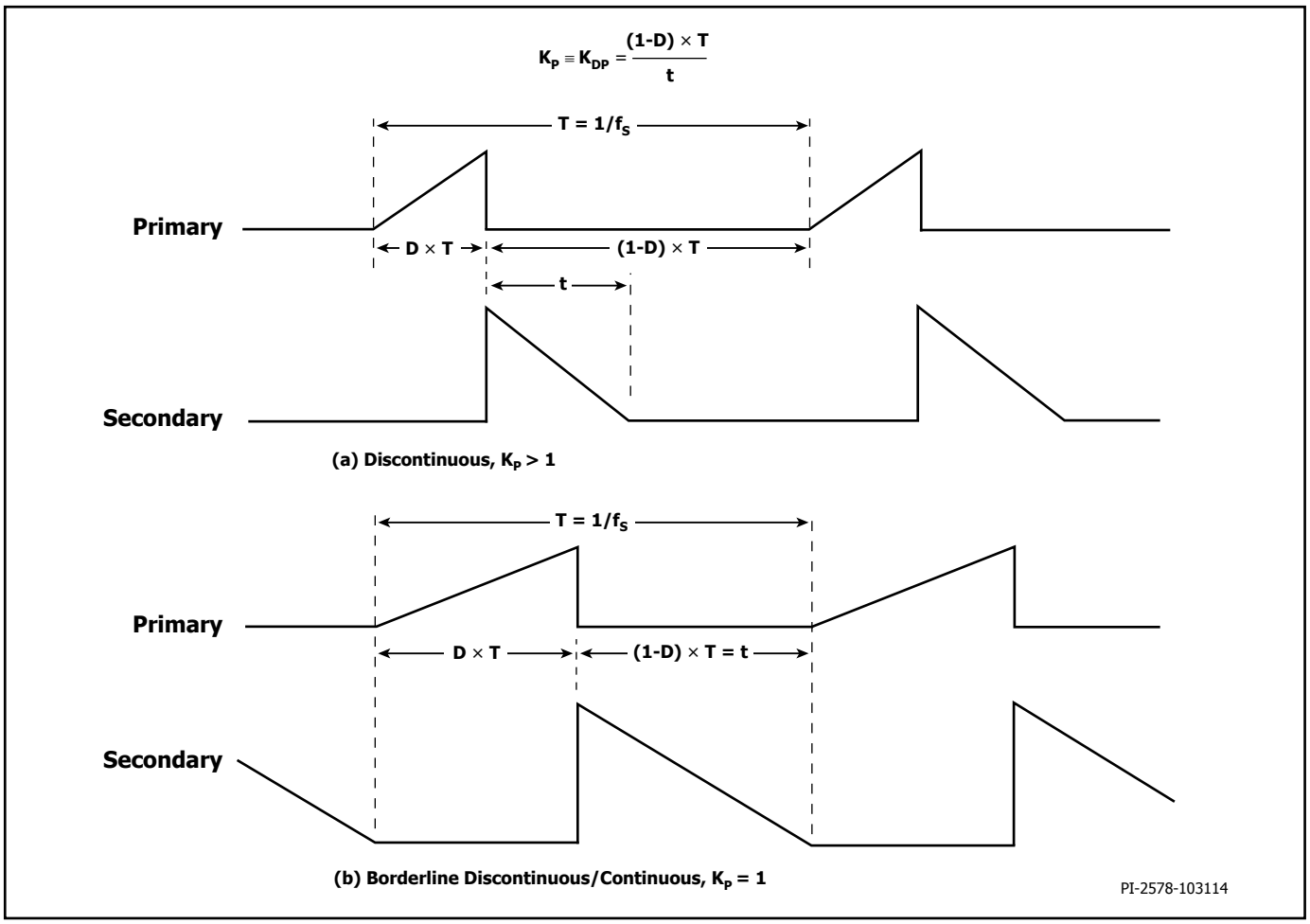


Figure 18. Discontinuous Conduction Mode Current Waveform, $K_p > 1$.

Quick Design Checklist

As with any power supply, the operation of all InnoSwitch3-AQ designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions.

As a minimum, the following tests are strongly recommended:

1. Maximum Drain Voltage – Verify that V_{DS} of InnoSwitch3-AQ and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Under all conditions, the maximum drain current for the primary switch should be below the specified absolute maximum ratings. At each input voltage condition and corresponding minimum and maximum load points, verify the leading edge current spike event duration is <200 ns. This is to ensure that the current limit is not falsely triggered. Longer duration indicates either excessive primary capacitance and/or output rectifier/clamp diodes with excessive reverse recovery time.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for InnoSwitch3-AQ IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of the InnoSwitch3-AQ IC.

Design Considerations When Using PowiGaN Devices (INN3997CQ, INN3999CQ and INN3990CQ)

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 19.

V_{OR} is the reflected output voltage across the primary winding when the secondary is conducting. V_{BUS} is the DC voltage connected to one end of the transformer primary winding.

In addition to V_{BUS}+V_{OR}, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch.

V_{CLM} in Figure 19 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of V_{BUS}, V_{OR} and V_{CLM}.

V_{OR} and the clamp voltage V_{CLM} should be selected such that the peak drain voltage is lower than 725 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during input transients will maintain the peak drain voltage well below 900 V.

To make full use of valley switching capability and ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.8 at minimum input voltage for universal input and $K_P \geq 1$ for high-line-only conditions.

Consider the following for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given PowiGaN INN3997CQ, INN3999CQ and INN3990C device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR FETs.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents the V_{OR} should be reduced to get highest efficiency. For output voltages above 15 V, V_{OR} should be maintained higher to maintain an acceptable PIV across the output synchronous rectifier.

V_{OR} choice will affect the operating efficiency and should be selected carefully. Table below shows the typical range of V_{OR} for optimal performance:

Output Voltage	Optimal Range for V_{OR}
5 V	45 - 70
12 V	80 - 120
15 V	100 - 135
20 V	120 - 150
24 V	135 - 180

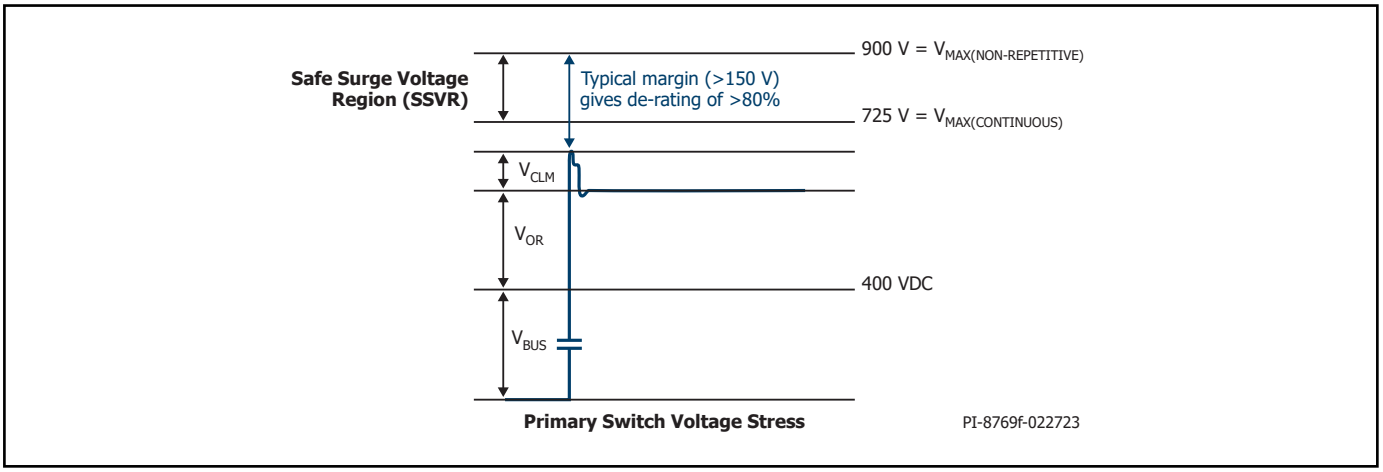


Figure 19. Peak Drain Voltage 900 V PowiGan Device for 400 VDC Input Voltage.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage:
- INN3977CQ ..... -0.3 V to 750 V
- INN3996CQ ..... -0.3 V to 900 V
- PowiGaN Device INN3997CQ ..... -0.3 V to 900 V[9]
- PowiGaN Device INN3999CQ ..... -0.3 V to 900 V[9]
- PowiGaN Device INN3990CQ ..... -0.3 V to 900 V[9]
- INN3947CQ ..... -0.3 V to 1700 V
- INN3949CQ ..... -0.3 V to 1700 V
- INN3947FQ ..... -0.3 V to 1700 V
- INN3949FQ ..... -0.3 V to 1700 V

DRAIN Pin Peak Current:
- INN3977CQ ..... 5.92 A[3]
- INN3996CQ ..... 5.72 A[4]
- PowiGaN Device INN3997CQ ..... 3.2 A[5]
- PowiGaN Device INN3999CQ ..... 10 A[5]
- PowiGaN Device INN3990CQ ..... 14 A[5]
- INN3947CQ ..... 5 A[5]
- INN3949CQ ..... 10 A[5]
- INN3947FQ ..... 5 A[5]
- INN3949FQ ..... 10 A[5]

VOLTAGE Pin Voltage:
- INN3977CQ ..... -0.3 V to 650 V
- INN3996CQ ..... -0.3 V to 650 V
- PowiGaN Device INN3997CQ ... -0.3 V to 650 V
- PowiGaN Device INN3999CQ ... -0.3 V to 650 V
- PowiGaN Device INN3990CQ ... -0.3 V to 650 V
- INN3947CQ ..... -0.3 V to 650 V
- INN3949CQ ..... -0.3 V to 650 V
- INN3947FQ ..... -0.3 V to 650 V
- INN3949FQ ..... -0.3 V to 650 V

VOLTAGE Pin Current ..... 200 µA[10]
BPP/BPS Pin Voltage ..... -0.3 to 6 V
BPP/BPS Pin Current ..... 100 mA
FWD Pin Voltage ..... -1.5 V to 150 V
SR, FB Pin Voltage ..... -0.3 V to 6 V
VOUT Pin Voltage ..... -0.3 V to 27 V
IS Pin Voltage ..... -0.3 V to 0.3 V[8]
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[6] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 125 °C
Lead Temperature[7] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Please refer to Figure 20 about maximum allowable voltage and current conditions.
4. Please refer to Figure 27 about maximum allowable voltage and current conditions.
5. Please refer to Figure 35 and 40 about maximum allowable voltage and current conditions.
6. Normally limited by internal circuitry.
7. 1/16" from case for 5 seconds.
8. Absolute maximum voltage for less than 500 µsec is 3 V.
9. PowiGaN devices:
   Maximum continuous drain voltage ..... -0.3 to 725 V.
   Maximum drain voltage (non repetitive pulse) ..... -0.3 to 900 V.
10. INN3947CQ, INN3949CQ, INN3947FQ, INN3949FQ, INN3997CQ, INN3999CQ, INN3990CQ only.

Thermal Resistance

Thermal Resistance: INN3977CQ, INN3996CQ, INN3997CQ, INN3999CQ and INN3990CQ
- (θ_{JA}) ..... 76 °C/W[1], 65 °C/W[2]
- (θ_{JC}) ..... 8 °C/W[3]

INN3947CQ
- (θ_{JA}) ..... 92 °C/W[1], 64 °C/W[2]
- (θ_{JC}) ..... 19 °C/W[3]

INN3949CQ
- (θ_{JA}) ..... 76 °C/W[1], 70 °C/W[2]
- (θ_{JC}) ..... 11 °C/W[3]

INN3947FQ
- (θ_{JA}) ..... 74 °C/W[1], 68 °C/W[2]
- (θ_{JC}) ..... 13 °C/W[3]

INN3949FQ
- (θ_{JA}) ..... 56 °C/W[1], 52 °C/W[2]
- (θ_{JC}) ..... 9.5 °C/W[3]

Notes:
1. Soldered to 0.36 sq. inch (232 mm²) 2 oz. (610 g/m²) copper clad.
2. Soldered to 1 sq. inch (645 mm²), 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Start-Up Switching Frequency	f_{SW}	T_J = 25 °C		23	25	27	kHz
				20.5		28.5	
Jitter Frequency	f_M	f_{SW} = 100 kHz T_J = 25 °C		0.8	1.25	1.7	kHz
Maximum On-Time	$t_{ON(MAX)}$		T_J = 25 °C	12.4	14.6	16.9	µs
				11.75		17.75	
		INN3947FQ/INN3949FQ	T_J = 25 °C	12.2	14.6	16.9	
				11.75		17.75	
BPP Supply Current	I_{S1}	INN3977CQ, INN3996CQ, V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching)	T_J = 25 °C	145	200	425	µA
				130		489	
		INN3947CQ, INN3949CQ V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching)	T_J = 25 °C	145	266	425	
				130		489	
		INN3947FQ, INN3949FQ V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching)	T_J = 25 °C	145	266	425	
				130		489	
		INN3997CQ, INN3999CQ, INN3990CQ V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching)	T_J = 25 °C	145	200	425	
				130		489	
	I_{S2}	INN3977CQ V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz)	T_J = 25 °C	0.9	1.20	1.73	mA
				0.85		2.00	
		INN3996CQ V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz)	T_J = 25 °C	0.7	0.9	1.35	mA
				0.63		1.5	
		INN3997CQ V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz)	T_J = 25 °C	0.93	1.24	1.79	mA
				0.8		1.9	
		INN3999CQ V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz)	T_J = 25 °C	1.7	1.95	2.5	mA
				1.6		2.6	
		INN3990CQ V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz)	T_J = 25 °C	1.7	1.95	2.5	mA
				1.6		2.6	
		INN3947CQ V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz)	T_J = 25 °C	0.93	1.25	1.8	mA
				0.8		1.9	
		INN3949CQ V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz)	T_J = 25 °C	1.46	1.95	2.81	mA
				1.26		3.0	
		INN3947FQ V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz)	T_J = 25 °C	0.93	1.25	1.8	mA
				0.8		1.9	
		INN3949FQ V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz)	T_J = 25 °C	1.46	1.95	2.81	mA
				1.26		3.0	
BPP Pin Charge Current	I_{CH1}	V_{DS} = 30 VDC	V_{BP} = 0 V, T_J = 25 °C	-1.75	-1.35	-0.88	mA
	I_{CH2}		V_{BP} = 4 V, T_J = 25 °C	-5.98	-4.65	-3.32	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
BPP Pin Voltage	V_{BPP}			4.65	4.90	5.2	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.39		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		5.15	5.36	5.65	V
		INN3947FQ/ INN3949FQ	I_{BPP} = 2 mA	5	5.36	5.65	
BPP Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.8	3.15	3.5	V
				2.1		4.13	
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF, See Note C	I_{LIMIT}	INN3977CQ di/dt = 300 mA/µs	T_J = 25 °C	1233	1326	1419	mA
		INN3996CQ di/dt = 238 mA/µs	T_J = 25 °C	1162	1250	1338	
		INN3997CQ di/dt = 325 mA/µs	T_J = 25 °C	1209	1300	1392	
		INN3999CQ di/dt = 425 mA/µs	T_J = 25 °C	1767	1900	2033	
		INN3990CQ di/dt = 525 mA/µs	T_J = 25 °C	2139	2300	2461	
		INN3947CQ di/dt = 300 mA/µs	T_J = 25 °C	1488	1600	1712	
				1440		1760	
		INN3949CQ di/dt = 425 mA/µs	T_J = 25 °C	1767	1900	2033	
				1710		2090	
		INN3947FQ di/dt = 300 mA/µs	T_J = 25 °C	1488	1600	1712	
				1408		1792	
		INN3949FQ di/dt = 425 mA/µs	T_J = 25 °C	1767	1900	2033	
				1672		2128	
Increased Current Limit (BPP) Capacitor = 4.7 µF, See Note C	$I_{LIMIT+1}$	INN3977CQ di/dt = 300 mA/µs	T_J = 25 °C	1385	1523	1662	mA
		INN3996CQ di/dt = 238 mA/µs	T_J = 25 °C	1319	1450	1581	
		INN3997CQ di/dt = 325 mA/µs	T_J = 25 °C	1343	1460	1577	
		INN3999CQ di/dt = 425 mA/µs	T_J = 25 °C	1980	2130	2279	
		INN3990CQ di/dt = 525 mA/µs	T_J = 25 °C	2395	2576	2756	
		INN3947CQ di/dt = 300 mA/µs	T_J = 25 °C	1674	1800	1926	
				1620		1980	
		INN3949CQ di/dt = 425 mA/µs	T_J = 25 °C	1980	2130	2279	
				1917		2343	
		INN3947FQ di/dt = 300 mA/µs	T_J = 25 °C	1674	1800	1926	
				1584		2016	
		INN3949FQ di/dt = 425 mA/µs	T_J = 25 °C	1980	2130	2279	
				1874		2385	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note B			200		ns
Current Limit Delay Time	t_{ILD}	T_J = 25 °C See Note B			120		ns
Overload Detection Frequency	f_{OVL}	T_J = 25 °C See Note A		102	110	118	kHz
		INN3947FQ/ INN3949FQ	T_J = 25 °C See Note A	101	110	118	
BYPASS Pin Auto-Restart Shutdown Threshold Current	I_{SD}	T_J = 25 °C		6	8.9	11.3	mA
				5.2		12	
Auto-Restart On-Time	t_{AR}	T_J = 25 °C		75	82	89	ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	See Note A	T_J = 25 °C		1.3		s
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C		1.7		2.11	s
		INN3947FQ/ INN3949FQ	T_J = 25 °C	1.7		2.15	
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C See Note B			0.2		s
Line Fault Protection for INN3977CQ & INN3996CQ							
VOLTAGE Pin Line Overvoltage Deglitch Filter	t_{OV+}	See Note B			3		µs
VOLTAGE Pin Voltage Rating	$V_{V(BVDSS)}$	T_J = 25 °C		650			V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C		23.9	26.1	28.2	µA
				22.1		30.4	
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C		21.5	23.7	25.5	µA
				19.7		27	
Brown-Out Delay Time	t_{UV+}	T_J = 25 °C			32		ms
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C		100	115	122	µA
				98		127	
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C		6	7	8	µA
				5		9.5	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Line Fault Protection for INN3947CQ & INN3949CQ						
VOLTAGE Pin Voltage Rating	$V_{V(BVDSS)}$	T_J = 25 °C	100			V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C	22.4	24.4	26.7	µA
			21.4		27.7	
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C	19	21.6	23.5	µA
			18		24.5	
Brown-Out Delay Time	t_{UV-}	T_J = 25 °C	29.7	35	40.5	ms
Line Fault Protection for INN3997CQ, INN3999CQ, INN3990CQ,						
Remote Disable Deglitch Filter	t_{OV+}	See Note B		3		µs
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C	110	115	122	µA
			98		127	
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C	6	8	9	µA
			5		10	
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C	23.9	26.1	28.2	µA
			22.1		30.4	
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C	21	23.7	25.5	µA
			19.7		27	
Brown-Out Delay Time	t_{UV+}			32		ms
Line Fault Protection for INN3947FQ, INN3949FQ						
VOLTAGE Pin Voltage Rating	$V_{V(BVDSS)}$	T_J = 25 °C	100			V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C	23.5	26.1	28.2	µA
			22.1		30.4	
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C	20.7	23.7	25.5	µA
			19.5		27	
Brown-Out Delay Time	t_{UV-}	T_J = 25 °C	28	35	40.5	ms
			25		44.4	
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C	110	115	122	µA
			98		127	
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C	6	8	9	µA
			5		10	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	INN3977CQ $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.20	1.38	Ω
			T_J = 125 °C		1.86	2.30	
		INN3996CQ $I_D = I_{LIMIT+1}$	T_J = 25 °C		2.35	2.8	
			T_J = 125 °C		3.4	4.5	
		INN3997CQ $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.97	1.56	
			T_J = 125 °C		1.6	2.38	
		INN3999CQ $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 125 °C		0.49	0.7	
		INN3990CQ $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 125 °C		0.41	0.61	
		INN3947CQ $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.2	1.53	
			T_J = 125 °C		2.2	3.12	
		INN3949CQ $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.45	0.62	
			T_J = 125 °C		0.77	1.1	
		INN3947FQ $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.2	1.53	
			T_J = 125 °C		2.2	3.12	
		INN3949FQ $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.45	0.62	
			T_J = 125 °C		0.77	1.1	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 80% BV_{DSS}				200	µA
Breakdown Voltage	BV_{DSS}	T_J = 25 °C	INN3977CQ	750			V
			INN3996CQ INN3997CQ INN3999CQ INN3990CQ	900			
			INN3947CQ, INN3947FQ	1700			
			INN3949CQ, INN3949FQ	1700			
Drain Supply Voltage		See Note A		30			V
Thermal Shutdown	T_{SD}	See Note A			142		°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			30		°C
Secondary							
FEEDBACK Pin Voltage	V_{FB}	T_J = 25 °C		1.235	1.265	1.29	V
				1.215		1.31	
		INN3947FQ/ INN3949FQ	T_J = 25 °C	1.235	1.265	1.29	
				1.215		1.313	
Maximum Switching Frequency	f_{SREQ}	T_J = 25 °C		118	132	145	kHz
FEEDBACK Pin Auto-Restart Threshold	$V_{FB(AR)}$				90		%
		See Note D			3.45		V
Output Voltage Pin Auto-Restart Timer	$t_{FB(AR)}$ $t_{IS(AR)}$	T_J = 25 °C			49.5		ms

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Secondary (cont.)							
BPS Pin Current at No-Load	I_{SNL}	T_J = 25 °C			280	485	µA
BPS Pin Voltage	V_{BPS}			4.20	4.40	4.60	V
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)(TH)}$			3.60	3.80	4.00	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)(H)}$				0.65		V
Current Limit Voltage Threshold	$I_{SV(TH)}$	Set By External Resistor		33.94		38	mV
FWD Pin Breakdown Voltage	V_{FWD}			150			V
Minimum Off-Time	$t_{OFF(MIN)}$			2.48	3.38	4.37	µs
Soft-Start Frequency Ramp Time	$t_{SS(RAMP)}$	T_J = 25 °C		7.5	11.75	19	ms
		INN3947FQ/ INN3949FQ	T_J = 25 °C	7.2	11.75	19	
BPS Pin Auto-Restart Shutdown Threshold Current	$I_{BPS(SD)}$			5.2	8.9	12	mA
FEEDBACK Pin Short-Circuit	$V_{FB(OFF)}$	T_J = 25 °C				135	mV
Synchronous Rectifier @ T_J = 25 °C							
SR Pin Drive Voltage	V_{SR}	T_J = 25 °C		4.2	4.4	4.6	V
SR Pin Voltage Threshold	$V_{SR(TH)}$	T_J = 25 °C			-3.3	0	mV
SR Pin Pull-Up Current	$I_{SR(PU)}$	T_J = 25 °C		135	165	195	mA
		T_J = -40 °C to 125 °C		100	165	230	
SR Pin Pull-Down Current	$I_{SR(PD)}$	T_J = 25 °C		260	298	336	mA
		T_J = -40 °C to 125 °C		186	298	435	
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2 nF	10-90% See Note B		40		ns
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2 nF	10-90% See Note B		15		ns
Output Pull-Up Resistance	R_{PU}	V_{BPS} = 4.4 V I_{SR} = 10 mA	T_J = 25 °C	7.2	8.5	9.6	Ω
			T_J = -40 °C to 125 °C	5	8.5	12.42	
Output Pull-Down Resistance	R_{PD}	V_{BPS} = 4.4 V I_{SR} = 10 mA	T_J = 25 °C	3.52	3.95	4.39	Ω
			T_J = -40 °C to 125 °C	2.35	3.95	6.72	

NOTES:

A. This parameter is derived from characterization.

B. This parameter is guaranteed by design.

C. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

D. See Feature Code Table (page 37) for optional variant.

Nominal BPP Pin Capacitor Value	Tolerance Relative to Nominal Capacitor Value	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	+100%

Typical Performance Curves

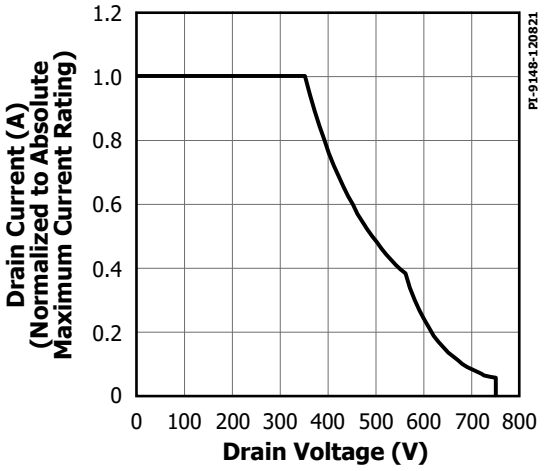


Figure 20. Maximum Allowable Drain Current vs. Drain Voltage (INN3977CQ).

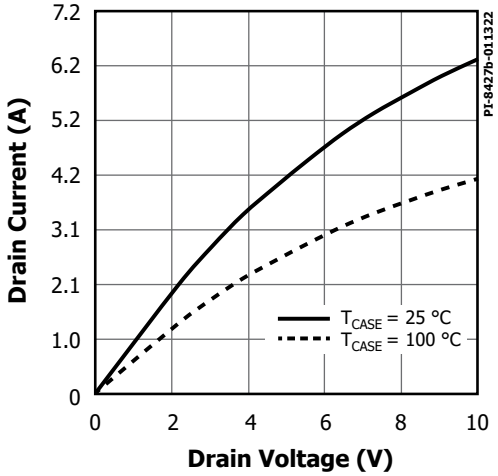


Figure 21. Output Characteristics (INN3977CQ).

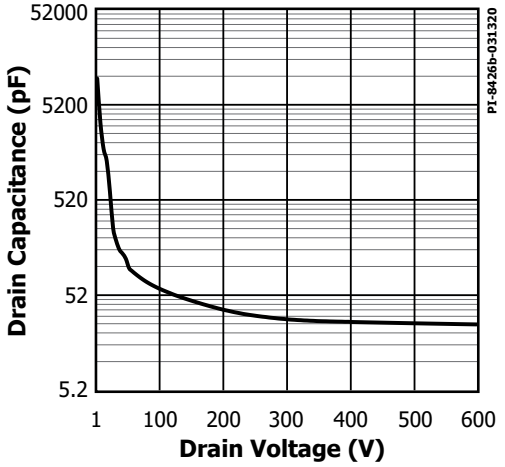


Figure 22. C_{OSS} vs. Drain Voltage (INN3977CQ).

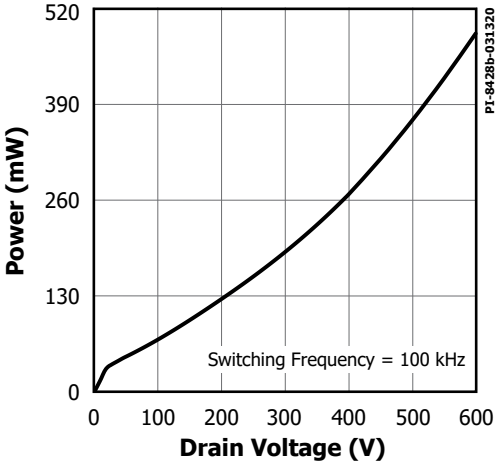


Figure 23. Drain Capacitance Power (INN3977CQ).

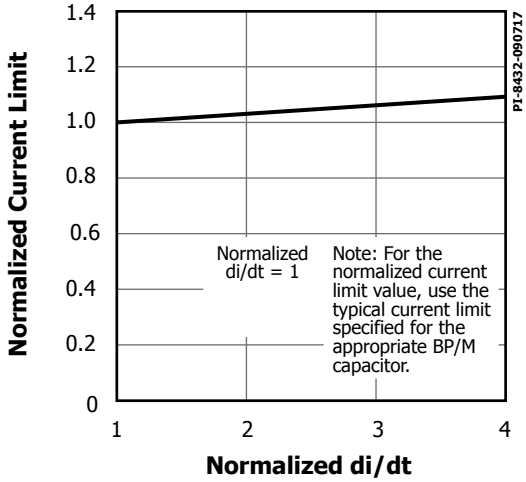


Figure 24. Standard Current Limit vs. di/dt.

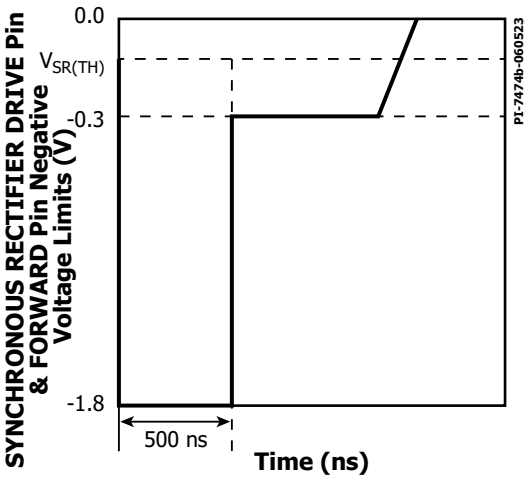


Figure 25. SYNCHRONOUS RECTIFIER DRIVE Pin and FORWARD Pin Negative Voltage Limits.

Typical Performance Curves

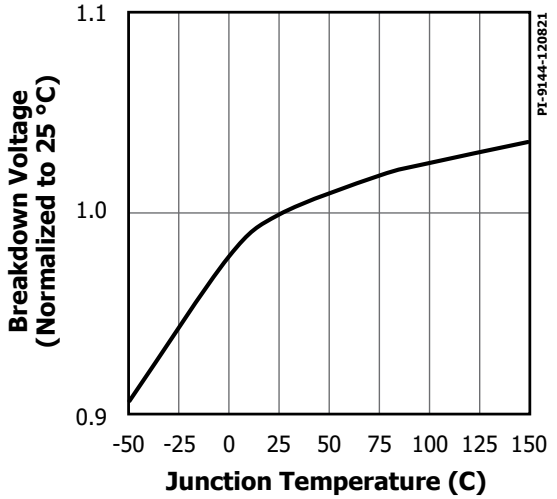


Figure 26. Breakdown Voltage vs. Temperature (INN3977CQ).

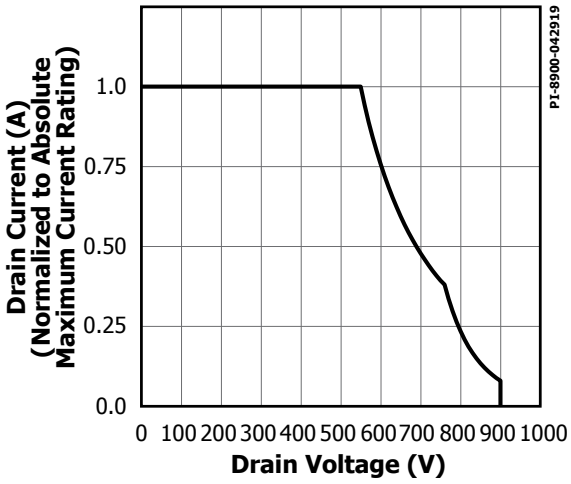


Figure 27. Maximum Allowable Drain Current vs. Drain Voltage (INN3996CQ).

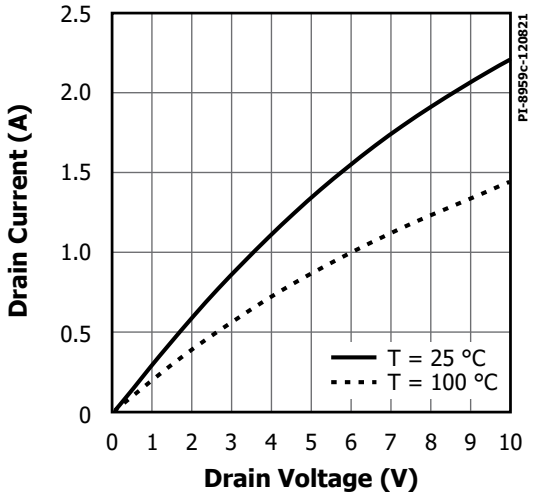


Figure 28. Output Characteristics (INN3996CQ).

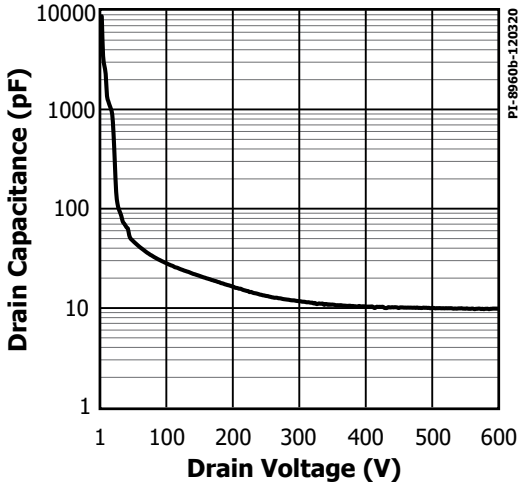


Figure 29. C_{OSS} vs. Drain Voltage (INN3996CQ).

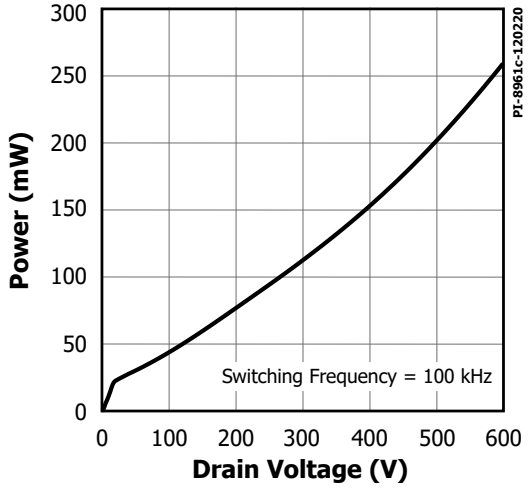


Figure 30. Drain Capacitance Power (INN3996CQ).

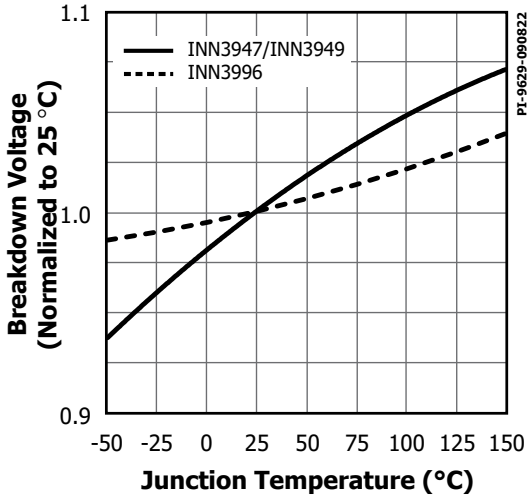


Figure 31. Breakdown Voltage vs. Temperature.

Typical Performance Curves

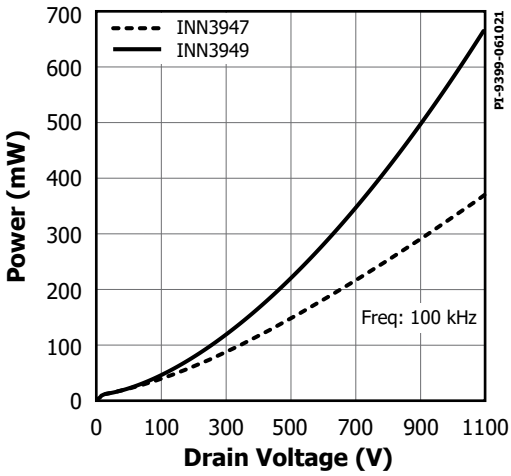


Figure 32. Drain Capacitance Power.

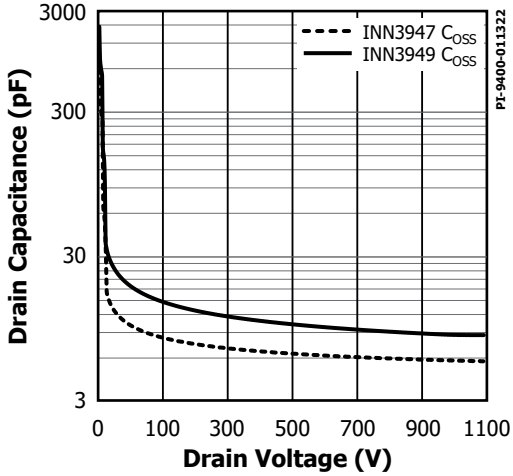


Figure 33. C_{OSS} vs. Drain Voltage.

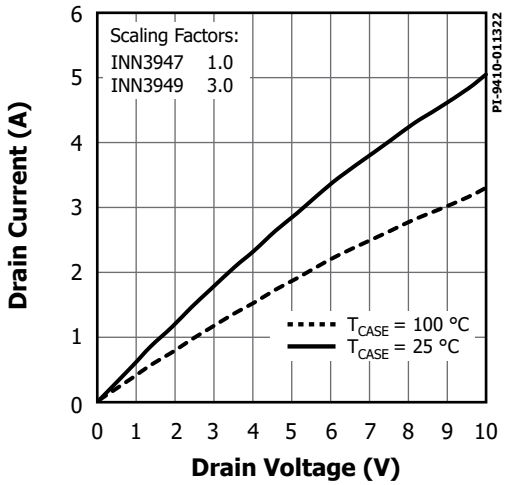


Figure 34. Output Characteristics.

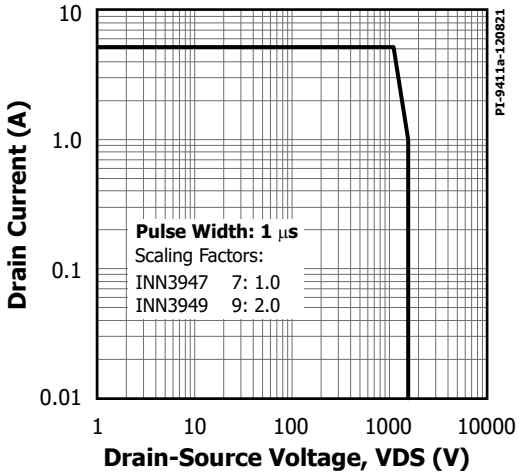


Figure 35. Maximum Allowable Drain Current vs. Drain Voltage.

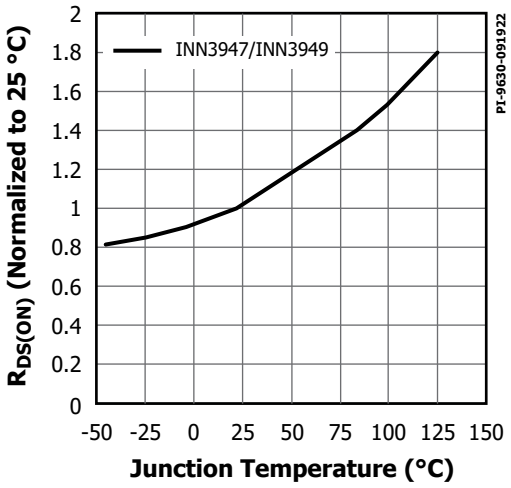


Figure 36. $R_{DS(ON)}$ vs. Temperature (INN3947/INN3949).

Typical Performance Curves

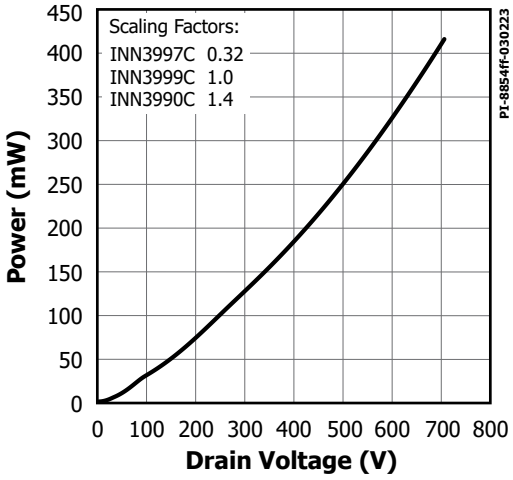


Figure 37. Drain Capacitance Power.

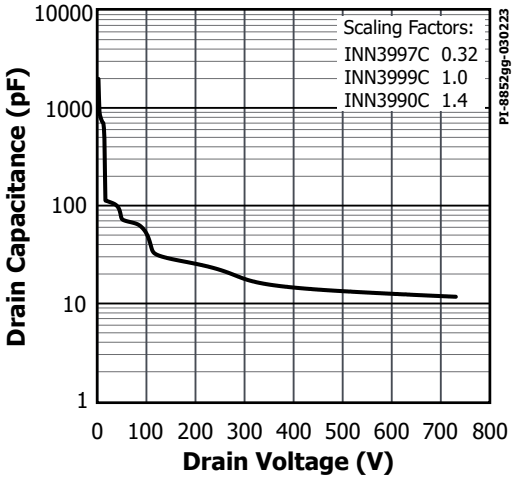


Figure 38. C_{OSS} vs. Drain Voltage.

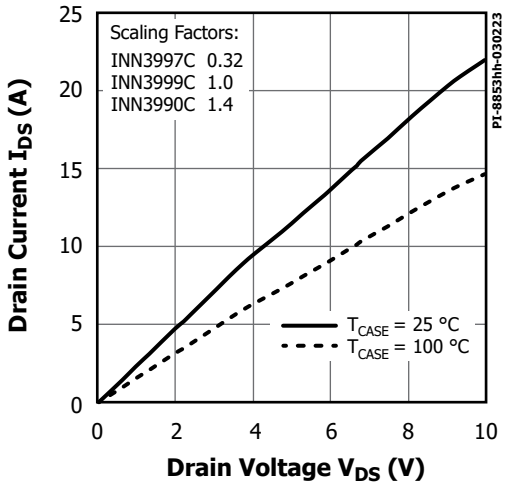


Figure 39. Output Characteristics.

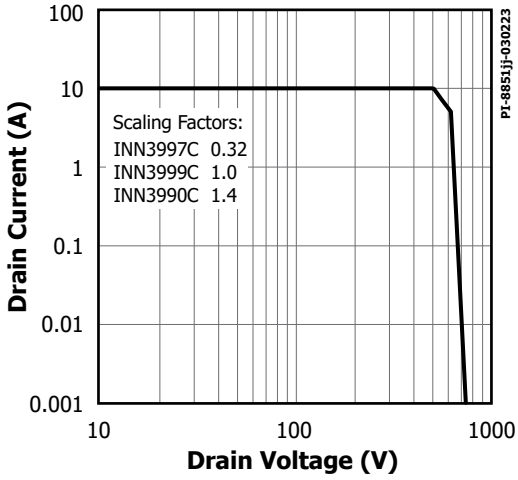
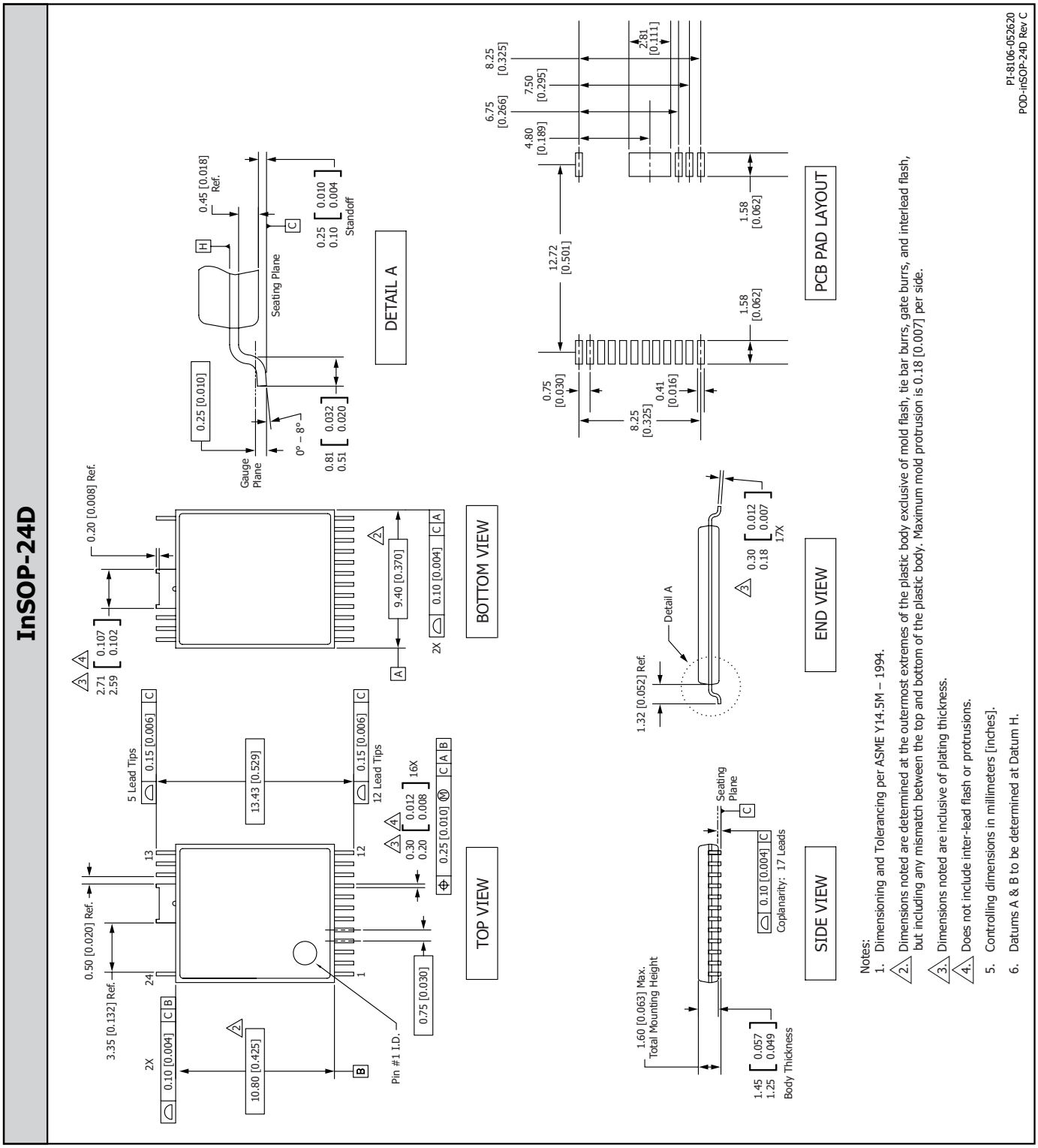


Figure 40. Maximum Allowable Drain Current vs. Drain Voltage.

InSOP-24D



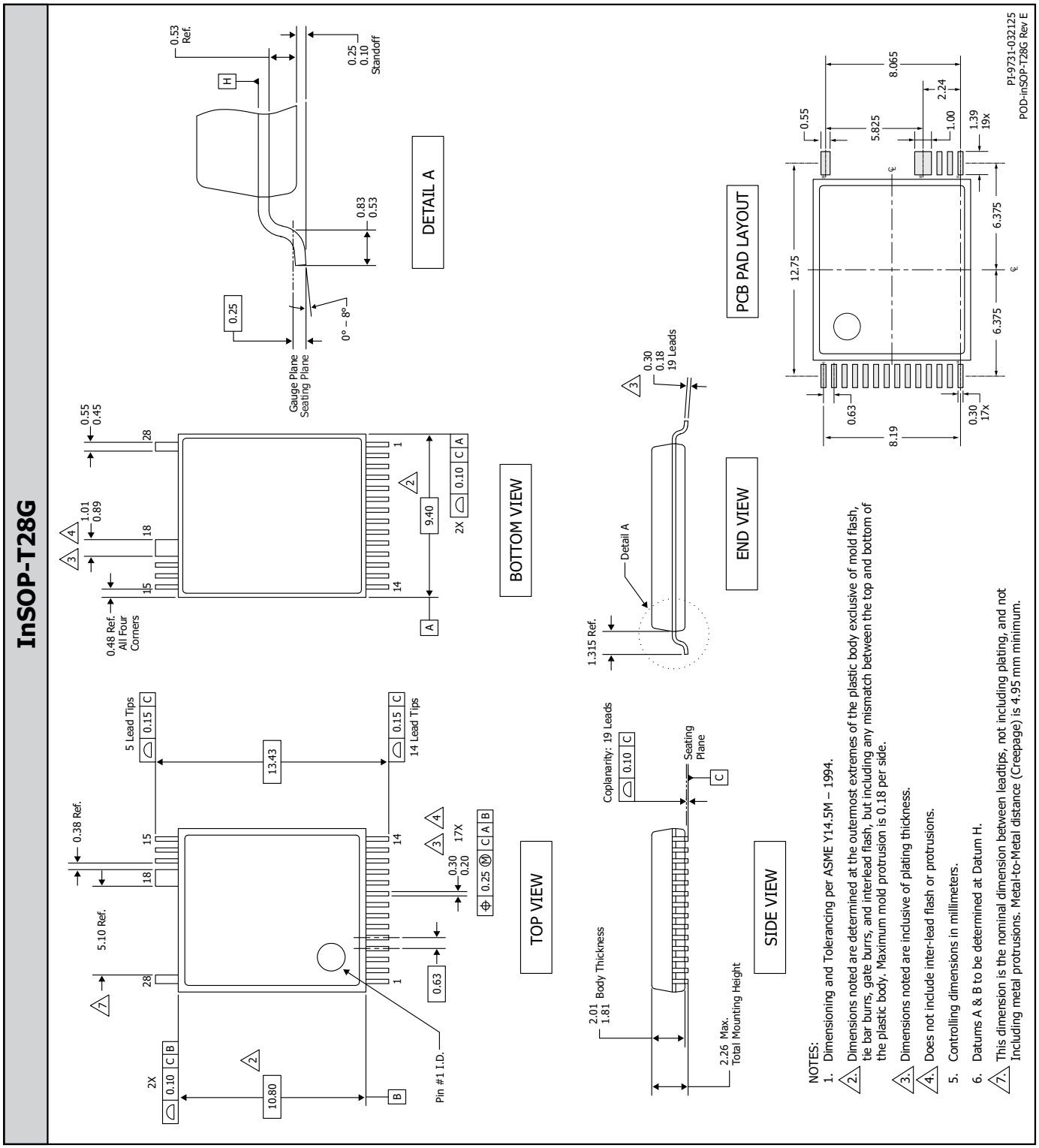
Notes:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters [inches].
6. Datums A & B to be determined at Datum H.

P1-8106-052620
POD-inSOP-24D Rev C

POD-inSOP-24D_C_052920

InSOP-T28G



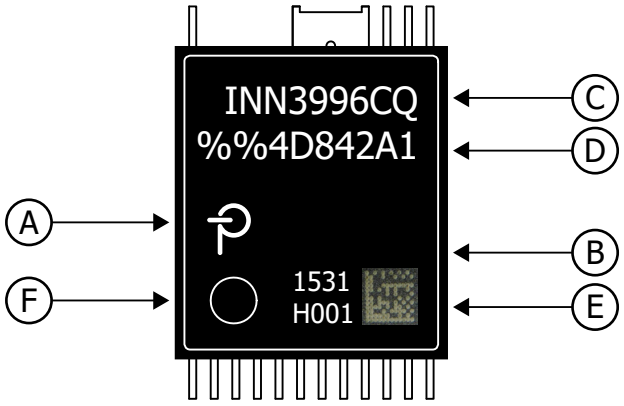
NOTES:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
7. This dimension is the nominal dimension between leadtips, not including plating, and not Including metal protrusions. Metal-to-Metal distance (Creepage) is 4.95 mm minimum.

P1-9731-032125
POD-inSOP-T28G Rev E
POD-inSOP-T28G_C_040423

PACKAGE MARKING

InSOP-24D

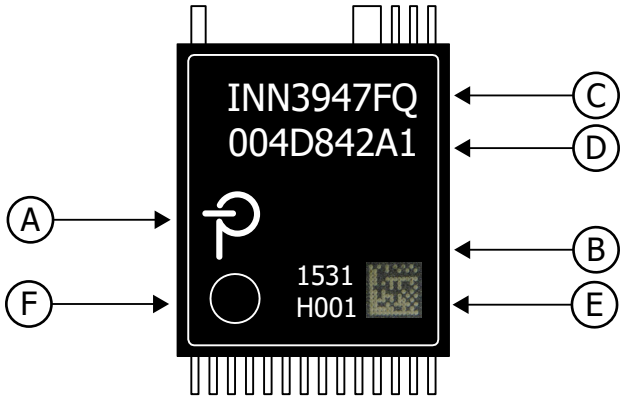


A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year (YY) followed by 2-digit work week (WW))
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Manufacturing Information Barcode
F. Pin 1 Indicator

PI-9413-070821

PACKAGE MARKING

InSOP-T28G



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year (YY) followed by 2-digit work week (WW))
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Manufacturing Information Barcode
F. Pin 1 Indicator

PI-9750-061623

Parameter	Conditions		Rating	Units
Ratings for UL1577				
Primary-Side Current Rating	Current from pin (16-19) to pin 24	INN3977CQ, INN3996CQ INN3997CQ, INN3999CQ, INN3990CQ	1.5	A
		INN3947CQ, INN3947FQ	0.65	
		INN3949CQ, INN3949FQ	1.1	
Primary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket resulting in T_{CASE} = 120 °C)		1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket)		0.125	W

Parameter	Symbol	Conditions		Rating	Units
Package Characteristics					
Clearance	CLR			11.4	mm (min)
Creepage	CPG			11.4	mm (min)
Distance Through Insulation	DTI			0.4	mm
Comparative Tracking Index	CTI			>600	V
Isolation Resistance, Input to Output	R_{IO}	V_{IO} = 500 V, T_J = 25 °C (See Note 1)		10^{12}	Ω (min)
		V_{IO} = 500 V, 100 °C ≤ T_J ≤ 125 °C (See Note 1)		10^{11}	
Isolation Capacitance, Input to Output	C_{IO}	(See Note 1)		1	pF
Package Insulation Characteristics					
Maximum RMS Working Isolation Voltage	$V_{IORM(RMS)}$	INN3977CQ		530	V_{RMS} (max)
		INN3996CQ, INN3997CQ, INN3999CQ, INN3990CQ		636	
		INN3947CQ, INN3947FQ, INN3949CQ, INN3949FQ		1202	
Maximum Repetitive Peak Isolation Voltage	$V_{IORM(PK)}$	INN3977CQ		750	V_{PK} (max)
		INN3996CQ, INN3997CQ, INN3999CQ, INN3990CQ		900	
		INN3947CQ, INN3947FQ, INN3949CQ, INN3949FQ		1700	
Maximum Transient Peak Isolation Voltage	V_{IOTM}	Test Voltage = V_{IOTM}, t = 60 s (qualification)		6.6	kV_{PK} (max)
		t = 1 s (100% production)		8	
Maximum Surge Isolation Voltage	V_{IOSM}	Surge Test 1.2/50 usec Table 2 IEC 60747-17		10.4	kV_{PK} (max)
Input to Output Test Peak Voltage	V_{PD}	Method A, After Environmental Tests Subgroup 1, V_{PD} = 1.6 × V_{IORM}, t = 10 s (qualification) Partial Discharge < 5 pC	INN3977CQ	1200	V_{PEAK} (min)
			INN3996CQ, INN3997CQ, INN3999CQ, INN3990CQ	1440	
			INN3947CQ, INN3947FQ, INN3949CQ, INN3949FQ	2720	
		Method A, After Input / Output Safety Test Subgroup 2/3, V_{PD} = 1.2 × V_{IORM}, t = 10 s, (qualification) Partial Discharge < 5 pC	INN3977CQ	900	
			INN3996CQ, INN3997CQ, INN3999CQ, INN3990CQ	1080	
			INN3947CQ, INN3947FQ, INN3949CQ, INN3949FQ	2040	
		Method B1, 100% Production Test, V_{PD} = 1.875 × V_{IORM}, t = 1 s Partial Discharge < 5 pC	INN3977CQ	1406	
			INN3996CQ INN3997CQ, INN3999CQ, INN3990CQ	1688	
			INN3947CQ, INN3947FQ, INN3949CQ, INN3949FQ	3188	
Insulation Resistance	R_S	V_{IO} = 500 V at T_J = 150 ºC		>10^9	Ω
Climatic Category				40/125/21	

Parameter	Conditions	Specifications
IEC 60664-1 Rating Table		
Basic Isolation Group	Material Group	I
Insulation Classification	Rated Mains RMS voltage ≤ 150 V	I - IV
	Rated Mains RMS voltage ≤ 300 V	I - IV
	Rated Mains RMS voltage ≤ 600 V	I - IV
	Rated Mains RMS voltage ≤ 1000 V	I - III

Note 1: All pins on each side of the barrier tied together creating a two-terminal device.

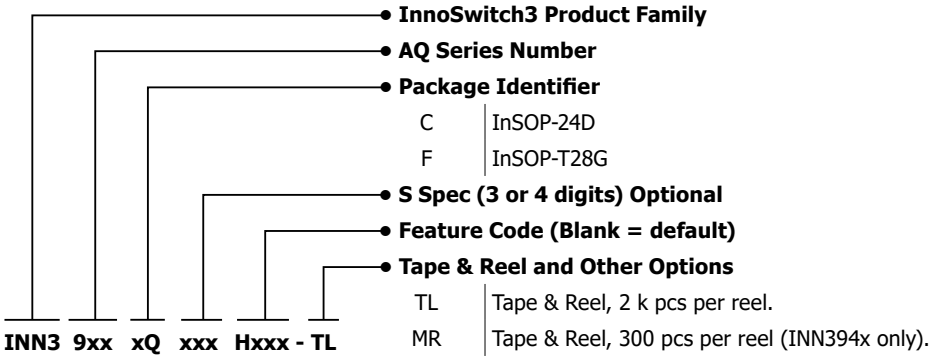
MSL Table

Part Number	MSL Rating
INN3977CQ	3
INN3996CQ	3
INN3997CQ	3
INN3999CQ	3
INN3990CQ	3
INN3947CQ	3
INN3949CQ	3
INN3947FQ	3
INN3949FQ	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information



Default Part ID List

Technology	BV_{DSS}	Part ID	S Spec	Feature Code	Default Controller Revision	Default Feature Code
Silicon	750 V	**INN3977CQ**	Blank	Blank	B60, > June 24, 2024	H640
	900 V	**INN3996CQ**				
PowiGaN	900 V	**INN3997CQ**	Blank	Blank	C4	H607
		INN3999CQ				
		INN3990CQ				
SiC	1700 V	**INN3947CQ**	Blank	Blank	C3, > June 21, 2024	H907
		INN3949CQ				
		INN3947FQ			C4	H607
		INN3949FQ				

Default part numbers (no S spec) are recommended for new designs. These automatically transition to future product revisions (after PCN period).

Feature Code Table

Feature Code	H100	H640	H607	H907
Default Feature Code	No	Yes		
Applicable Part ID	INN3949CQ INN3999CQ	INN3977CQ INN3996CQ	INN3997CQ INN3999CQ INN3990CQ INN3947FQ INN3949FQ	INN3947CQ INN3949CQ
Feedback	External			
Current Sense (I_S)	External			
Primary I_{LIM}	External			
Secondary Fault Response	Auto-Restart			
Auto-Restart Trigger	V_O < 3.45 V	V_O < 90%		
Over-Temperature Protection Behavior	Hysteretic			
V Pin Function	UV, OV	UV, OV	UV, OV	UV Only
V Pin UV Timer (t_{UV-})	32 ms			
VOUT Pin OVP Function	Enabled			
Peak Power Delivery Mode	Disabled			

Feature codes allow for modification of device functionality from the default. For default features it is not required to include the H code in the ordered part number. Only the H100 must be explicitly included with part ID INN3949C, INN3999C if the modified functionality is required.

Part Ordering Examples

INN3947FQ-TL	InnoSwitch3-AQ family, series number 947, InSOP-28G package, no S spec, tape and reel
INN3947CQ0501-TL	InnoSwitch3-AQ family, series number 947, InSOP-24D package, S spec for controller rev C, tape and reel
INN3949FQ502-MR	InnoSwitch3-AQ family, series number 949, InSOP-28G package, S spec for controller rev C4, mini tape and reel
INN3949CQ-H100-TL	InnoSwitch3-AQ family, series number 949, InSOP-24D package, no S spec, feature code H100, tape and reel

Specific Revision Part ID List

Family	Orderable Part ID with S Spec	Controller Revision	PCN Reference	Description
InnoSwitch3-AQ Si MOSFET	INN3977CQ0500	B60 (latest)	PCN-23181	Allow specific controller revisions to be specified
	INN3977CQ0501	B5	PCN-23181	Allow specific controller revisions to be specified
	INN3977CQ0510	B60 (latest)	PCN-23181	Only with 2D barcode marking and allow specific controller revisions to be specified
	INN3996CQ0500	B60 (latest)	PCN-23181	Allow specific controller revisions to be specified
	INN3997CQ0501	B5	PCN-23181	Allow specific controller revisions to be specified
InnoSwitch3-AQ SiC Switch	INN3947CQ0500	C3 (latest)	PCN-23231	Allow specific controller revisions to be specified
	INN3947CQ0501	C	PCN-23231	Allow specific controller revisions to be specified
	INN3949CQ0500	C3 (latest)	PCN-23181	Allow specific controller revisions to be specified
	INN3949CQ0501	C	PCN-23231	Allow specific controller revisions to be specified. Not available in H100 feature code
	INN3947FQ502	C4 (latest)	PCN-23231	Allow specific controller revisions to be specified
	INN3949FQ502	C4 (latest)	PCN-23231	Allow specific controller revisions to be specified
InnoSwitch3-AQ GaN Switches	N/A	N/A	N/A	N/A

Specific revision part IDs (with S Spec number) allows specifying:

- A device revision regardless of future changes
- A newer revision before PCN effective date of default part numbers

Revision	Notes	Date
D	Production release.	02/21
E	Production release of INN3947CQ and INN3949CQ.	01/22
F	Typical curves added for INN3947/INN3949: BV_{DSS} and $R_{DS(ON)}$.	10/22
G	Updated isolation voltage and DIN VDE V 0884-11 on page 1. Updated V_{IOTM} and deleted V_{ISO} on page 29.	11/22
H	Introduction release of INN3997CQ, INN3999CQ, INN3990CQ part numbers.	05/23
I	Added S Spec Table.	08/23
J	Added Feature Code Table.	11/23
K	Production release of 900 V PowiGaN, INN3997CQ, INN3999CQ, INN3990CQ part numbers.	12/23
L	Updated ABS Max Table, Note 10 page 18, and Part Ordering Information Table page 36.	01/24
M	Updated parameter values for I_{S2} INN3997CQ, $R_{DS(ON)}$ INN3997CQ and V_{FB}.	06/24
N	Updated Safety approval information on page 1.	09/24
O	Introduction release of INN3947FQ and INN3949FQ parts.	11/24
P	Preliminary release of F package parts.	12/24
Q	Added PCB Pad Layout to InSOP-T28G Package Drawing. Code A production release of F package with associated update of parameter table entries.	03/25
R	Correction to revision history for revision Q.	03/25
S	Release of 510 S-Spec for INN3977CQ.	06/25
T	Preliminary release of H100 Feature Code for INN3999CQ.	06/25
U	Introduction release of H100 Feature Code for INN3999CQ.	08/25
V	Production release of H100 Feature Code for INN3999CQ.	09/25

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